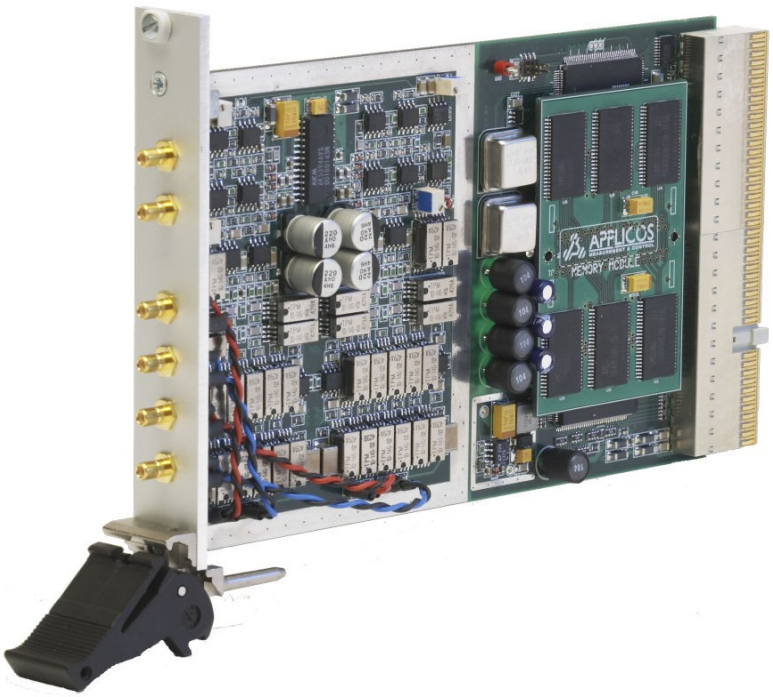
APPLICOS
MEASUREMENT & CONTROL

Hardware Manual

# PD24222

## DUAL 24BIT PXI WAVEFORM DIGITIZER

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PXI

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# 1 Introduction

The PD24222 is a two channel high accuracy 24-bit Waveform Digitizer intended for audio, telecom and vibration signal acquisition
The module has two selectable anti-aliasing input filters and an input gain amplifier with 10dB steps. The analog signal path from the two channels are complete separate so these settings can be set separate for each channel. The sample rate is software selectable to all commonly used audio sample rates. By applying an external clock the user can sample at any rate from 1 kHz up to 220 kHz Figure 1 shows the functional block diagram from the PD24222.

On the left side of the diagram are the differential analog inputs, the external clock in- /output and the trigger input. The analog input is a differential input. By switching one input to ground or to the programmable DC Offset source it becomes a single ended input with programmable DC mid level. The Trigger input allows the user to control the start of data capturing.
After the 24 bit analog to digital conversion there is the 1Mword RAM capture memory
When the PD24222 is triggered, the capture memory starts running from its start address. During the measurement an internal or external clock increments the memory counter. When the counter reaches the value of the stop address it jumps back to the start address, or stops if the loop mode is programmed off.
On the right side of the diagram there is the PXI interface to control the card.

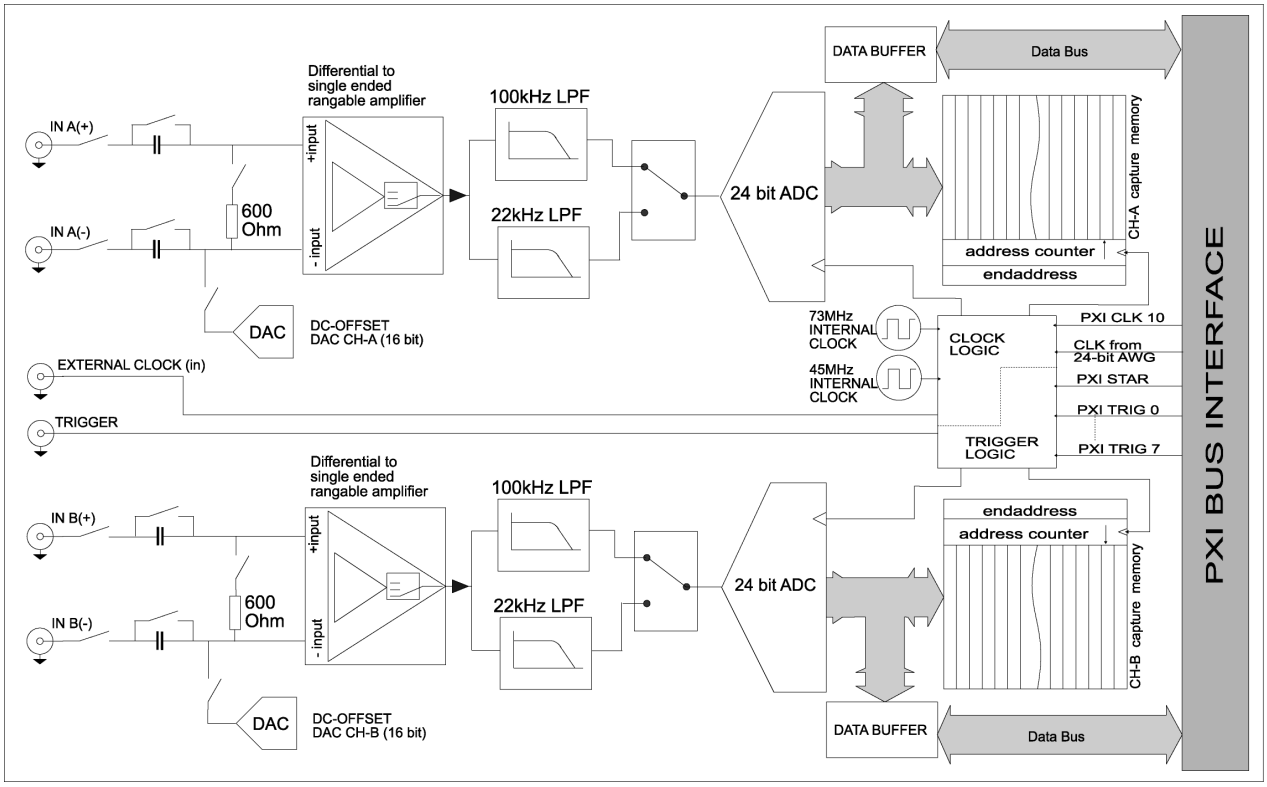


**Figure 1 PD24222 functional block diagram**

## 2 Analog circuit

The SMB connectors marked A+, A- ,B+ and B-, on the front of the PD24222, are the analog differential inputs for channel A and channel B. If a channel is set in the single input mode the negative input is connected to ground or to the programmable DC Offset source. The + input becomes a single ended input with programmable DC mid level. A gain amplifier stage on the inputs gives a gain selection from -20 to +30 dB in 10 dB steps.
**Important:** Be sure to tighten the small screws at the top and bottom of the front face of the PD24222 for a reliable ground connection.

### 2.1 Analog Input

Figure 2 shows the analog input circuit. The analog input impedance is selectable, 600 Ω or 1MΩ and the input coupling can be AC or DC.
If you select DC coupling, any DC offset present in the input signal is passed to the ADC. Use this coupling configuration if the signal source has a small amounts of offset voltage or if the DC content of the signal is important.
Select AC-coupling if the input signal has a DC component that you want to reject.
If the analog input is disconnected, the internal circuit is disconnected from the input by a mechanical switch. The settings for the input mode are separate for each channel,

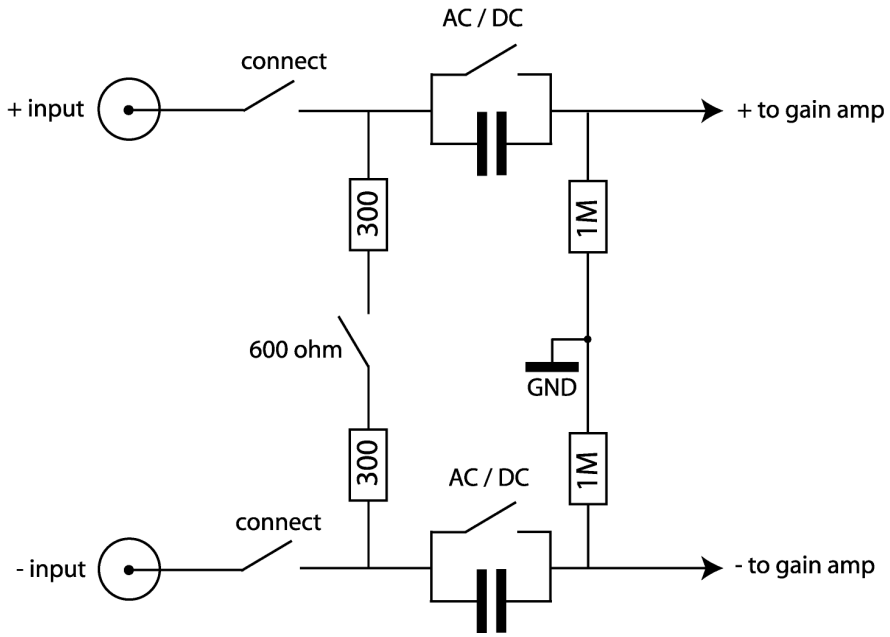


**Figure 2 PD24222 analog input circuit**

### 2.2 Input ranges:

The PD24222 offers six ranges to optimize the ADC resolution to the input signal.

| Input range | Gain |
|---|---|
| 10Vpp | 0dB |
| 3.16Vpp | 10dB |
| 1Vpp | 20dB |
| 316mVpp | 30dB |
| 100mVpp | 40dB |
| 31.6mVpp | 50dB |

**Table 1 Input ranges PD24222**

### 2.3 programmable DC Offset source

If a channel is set in the single input mode, the + input becomes the single ended input and the negative input is connected to Ground or to the programmable DC Offset source.
The programmable DC offset source is a 16 bit DAC with a range of +5Volt to –5Volt. When the input offset is used the negative connector from the differential input is disabled

***Example:*** Examine a signal (1Vpp) on a 1 Volt DC offset, see Figure 3. The top of the input signal is 1Volt offset + 0.5V signal = 1.5Vpeak input voltage. Without using input offset, you would need to specify a range of 3.16Vpp (-10 dB) to capture the waveform. In this case a large range from the ADC will not be used because of the DC voltage on the signal. However, with the input offset set to 1Volt, the signal center around 0V and a range of 1Vpp ( 0dB ) is enough to capture the signal. This improves the accuracy of the measurement.

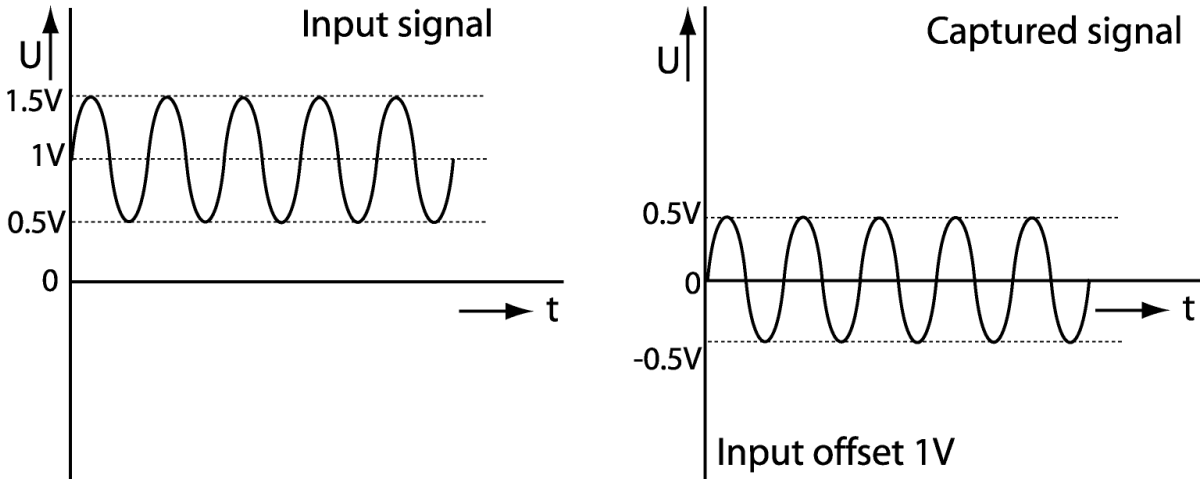


**Figure 3 Input offset**

### 2.4 Analog input filters

Each channel has two selectable 3-pole low pass filters. The filters limit the bandwidth of the signal path and is useful for rejecting out of band noise.
The selectable filters have cutoff frequencies of: 22kHz and 100kHz. Figure 4 shows the typical frequency response from the PD24222

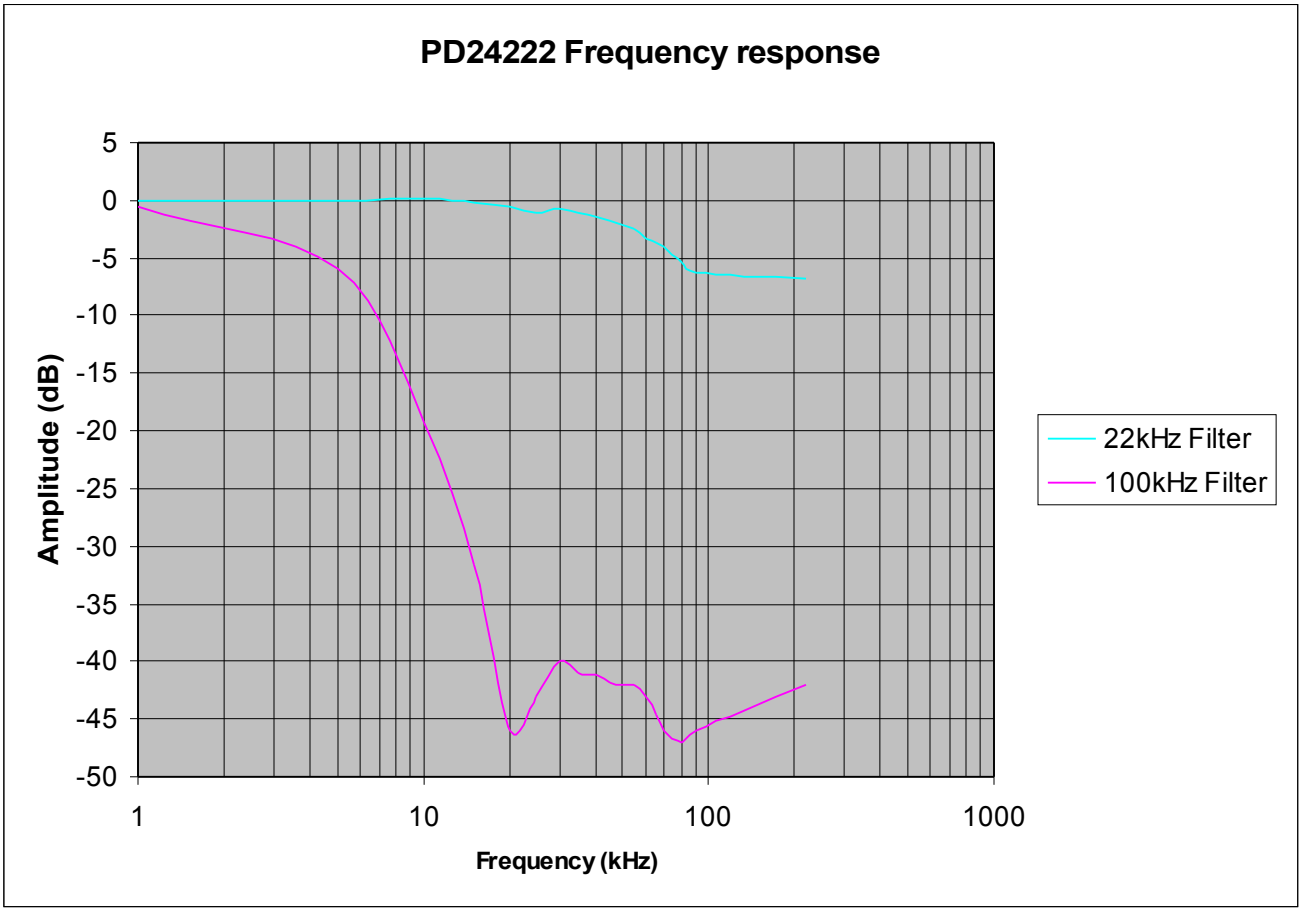


**Figure 4 Typical frequency response**

## 3 Clocking

The PD24222 can sample on five different clock sources, two internal and three external clock sources. The internal clock sources are two onboard crystal oscillators from 73.728 MHz and 45.1584 MHz. The external clock sources can be an external clock source connected to the front SMB connector or the 10 MHz PXI clock provided through the PXI connector.

If the digitizer is used in combination with the 24 bit arbitrary waveform generator* it is possible to synchronize both modules. The arbitrary waveform generator passes on the main clock through PXI local bus 0 to the PD24222. Notice this is the main clock frequency and not the update frequency from the arbitrary waveform generator. (undivided clock). If this synchronize option is used both modules must be placed next to each other and the waveform generator must be on the left side of the PD24222 digitizer.

To synchronize the PD24222 to other devices in a measurement system, an external sample clock can be connected on the front panel clock input. The front panel clock input has a 50-Ohm termination.

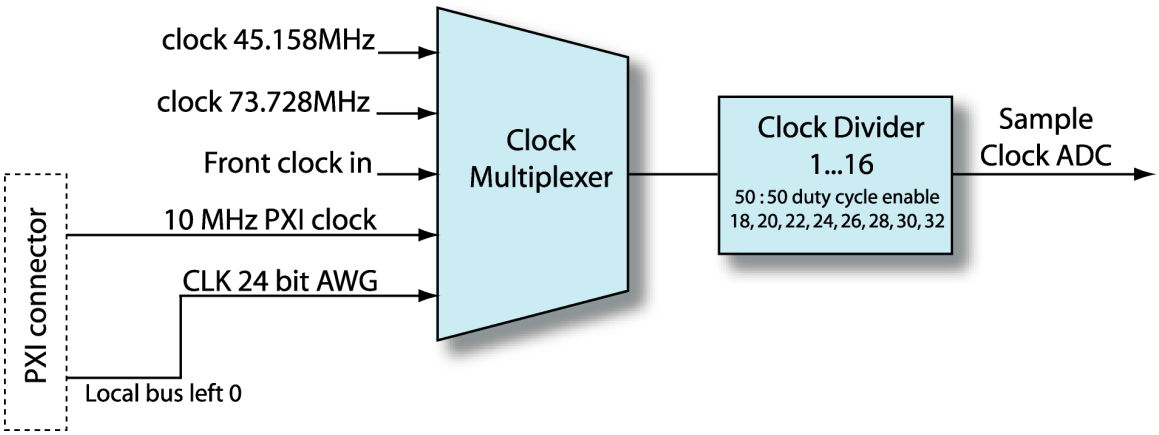


**Figure 5 PD24222 clock circuit**

### 3.1 Sample Rate

The sample rate is not only dependent on the clock source and clock divider, but also of the operation mode in which the AD converter chip operates. The ADC has three operation modes, see Table 2.

| Operation mode | Sample clock frequency |
|---|---|
| Normal | f sample = Clock / 256 |
| Double | f sample = Clock / 128 |
| Quad | f sample = Clock / 64 |

**Table 2 ADC operation modes**

The final sample rate depend on the Clock source, the clock divider and the ADC operation mode. The sample frequency can be derived by the following formula :

$$f_{sample} = \frac{f_{clock}}{a \cdot n}$$

***a*** = 64 for quad speed, 128 for double speed and 256 for normal speed operation;
***n*** = the divider value programmed by the user, *n* = 0 to 32

Here some examples from common used sample rates.

| Sample Rate (kHz) | Clock Source (MHz) | Clock divider | Master clock (MHz) | Sample clock frequency | Operation mode |
|---|---|---|---|---|---|
| 24 | 73,728 | 12 | 6,1440 | MasterClk / 256 | normal speed |
| 32 | 73,728 | 9 | 8,1930 | MasterClk / 256 | normal speed |
| 44,1 | 45,1584 | 4 | 11,2896 | MasterClk / 256 | normal speed |
| 48 | 73,728 | 6 | 12,2880 | MasterClk / 256 | normal speed |
| 96 | 73,728 | 6 | 12,2880 | MasterClk / 128 | double speed |
| 192 | 73,728 | 6 | 12,2880 | MasterClk / 64 | quad speed |

**Table 3 Examples of sample rates**

### 3.2 Digital high pass filter

The PD24222 includes a selectable digital high pass filter for DC offset cancellation. The cut-off frequency scales with the sampling rate. (see Table 4 ) At fsample = 48kHz in the normal speed mode, at fsample = 96kHz in the double speed mode and at fsample = 192kHz in the quad speed mode the cut-off frequency is 1Hz

| Operation mode | fc cut-off frequency |
|---|---|
| Normal | f sample / 48kHz |
| Double | f sample / 96kHz |
| Quad | f sample / 192 kHz |

**Table 4 High pass filter cut-off frequency**

### 3.3 Capture frequency

The AD converter chip has two AD converters in one chip, this means that channel A and B always have the same sample frequency. And the lowest possible sample frequency capture is limited to the minimum sample frequency from the ADC. (1 kS/s)

If you request a sample rate less than 1 kS/s or to capture with different sample frequencies it is possible to divide the capture clock to a lower frequency with the onboard capture divider. The capture divider stores only one sample in a group of *n* samples, effectively reducing the sample rate. The capture frequency can be derived by the following formula :

$$f_{capture} = \frac{f_{sample}}{n}$$

***f capture*** = the final sample rate (kS/s)
***f sample*** = clock source frequency (kS/s)
***n*** = capture divider value 1 to 16

Each channel has its own capture-divider, so they can capture on different frequencies.

***Example:*** A analog signal is connected to channel A and B. (see Figure 6) The ADC sample clock is 96kHz. The capture divider for channel A is set to 1 and for channel B it is set to 2.

The result is that the capture frequency for channel A is the same as the sample frequency from the ADC, but the capture frequency for channel B is halve the sample frequency.
Channel A has a sample frequency from 96kHz and channel B 48khz.

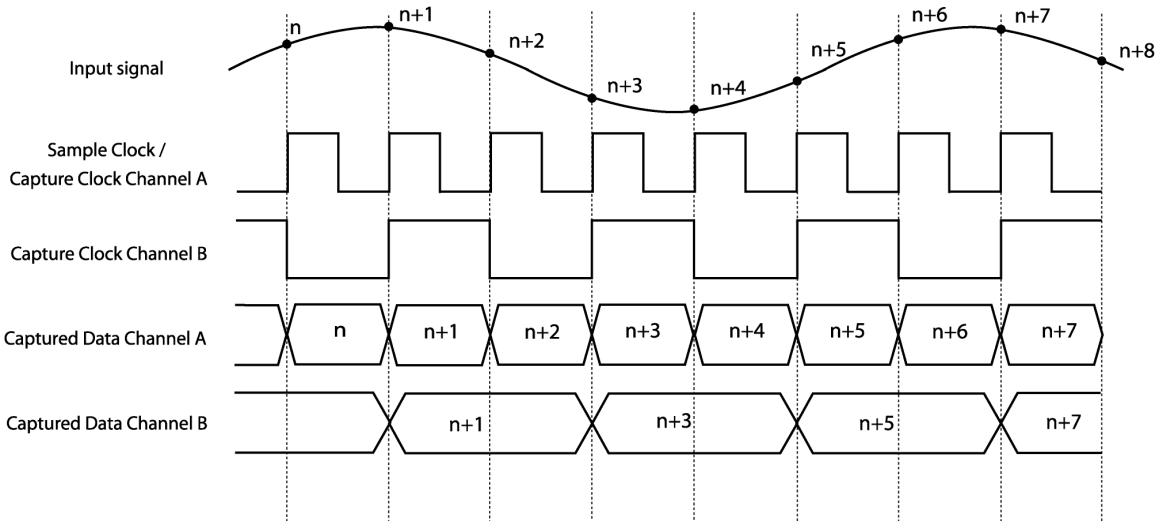


**Figure 6 Different capture frequency's**

# 4 Triggering

To prevent triggering during connection or initializing there is a “lock” bit.
After writing a logic ‘1’ into the lock bit in the PD24222 register, the PD24222 comes in the capture mode. In the capture mode the card is sensitive for a trigger event. The PD24222 can trigger on three trigger sources: Digital input trigger, Software trigger and Analog trigger.
The separate trigger circuits from Channel-A and Channel-B makes that each channel can start on different trigger sources and on different trigger edges or levels. Figure 7 shows the trigger capabilities.

## 4.1 Digital input triggering

The digital trigger accepts triggers from the front panel and from the PXI back plane including PXI TRIGGER 0 to 7 and PXI STAR TRIGGER. The front panel trigger input uses normal TTL logic levels, with a 0.5V nominal threshold for a low level and a 2V nominal threshold for a high level. All the trigger inputs except the software trigger can handle different trigger events. It is possible to trigger on positive and negative level or positive and negative edge trigger signals.
For settings see the *PD24222_SetTriggerInput* command in the **PD24222 driver manual.**
In level trigger mode the capturing starts when trigger goes active and stops when trigger goes inactive. Edge trigger mode has two options, normal or continuous. In normal mode the capturing starts at a trigger edge and either stops on the next trigger edge. In continuously mode the measurement runs until stopped by the software. Every measurement can be stopped with the software by forcing the channel out of “lock mode”. When the module is out of lock mode the trigger register will be cleared.

## 4.2 Software triggering

If trigger timing is not a issue, there is a software initiated trigger. By writing the trigger register the capturing can be started or stopped.

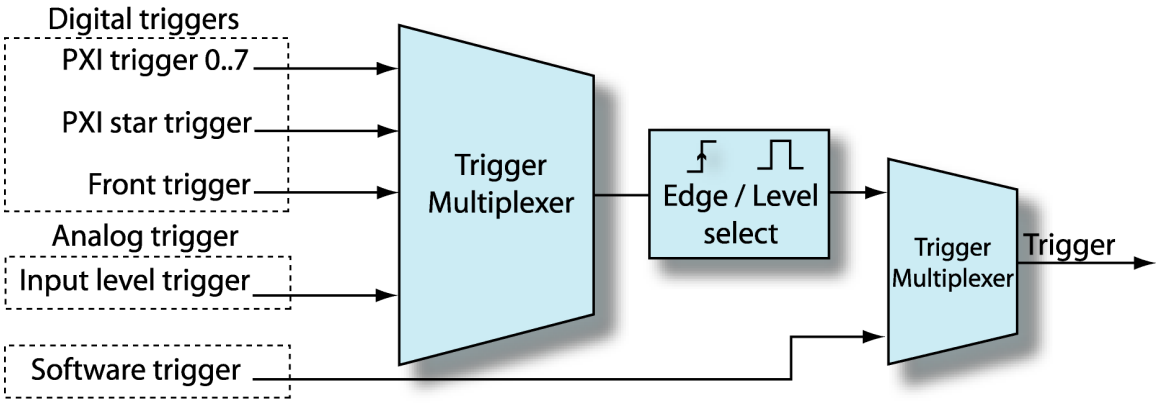


**Figure 7 PD24222 trigger capabilities**

## 5 Onboard Memory

The onboard memory is for the storage of the captured data before transfer to the computer. This capture memory has the size of 1M x 24 bit, available for each channel.
The capture memory of the PD24222 is addressed through a counter. This counter is active as well during capturing as during reading or writing the memory via the bus.

Before entering the capture mode “the mode were the card is sensitive for a trigger event”, the start address from the address counter must be set with the DLL *PD24222_SetAddressCounter.* ( see **PD24222 driver manual** )
After entering the capture mode, and a trigger event is occurred the measurement is started and the counter starts counting from the start address. The counter increments on each sample clock edge, until it reaches the end address from the memory ( FFFFF Hex ). At the end of the memory the counter stops, or jumps to address 00000 Hex and counts up again, see Figure 8. This depends on the setting of the loopmode bit. (DLL function *PD24222_SetLoopMode*.) Writing a logic “0” loopmode is disabled and writing a logic “1” loopmode is enabled.

After a measurement the memory can be read back in through the PXI interface.
In bus access mode the same counter mechanism is active except that the clock is now the read or write signal. Before a data read the start address must be written, so the counter is pointing to the address where the measurement is started. After each read or write the counter increments to the next address allowing burst read or write actions. Since the memory can not be read or written during pattern generation, there is a lock bit that should be set to allow pattern generation. The memory is then locked for reading or writing. After setting the lock bit to unlock the memory is accessible again. A measurement that was running at that moment will be aborted.

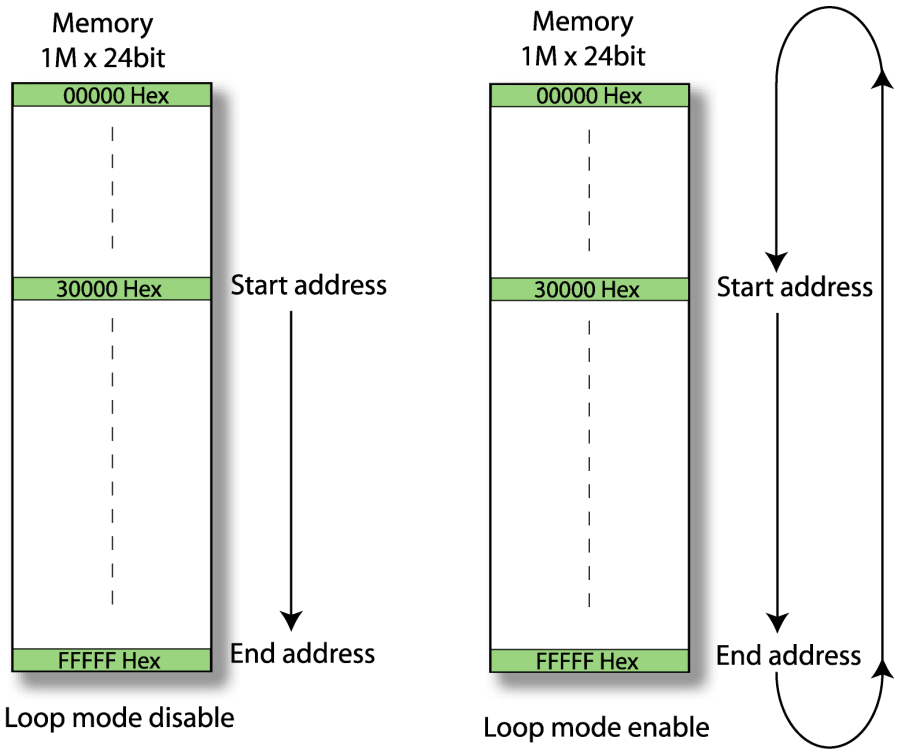


**Figure 8 Function of the loopmode bit**

# 6 Calibration

Calibration is a test that compares the values indicated by the PD24222 with a external reference source. The result of a calibration is used to determine the gain and offset error so the PD24222 can correct the error.
For optimum performance use self-calibration when the digitizer is placed in a new system or if the temperature changes more than 5°C from the previous calibration
The maximum recommended amount of time between two calibrations is six months.

The calibration can be done with the software tool **PD24222 calibration** or with the DLL function *PD242222_AutoCalibrate*.
The input offset DAC is used as reference voltage source. Before the auto calibration is started the input offset DAC must be calibrated first, using a calibrated high-precision voltmeter connected to the negative input.
Once the calibration process is done, the calibration constants will be stored in EEPROM. These values will be loaded by the software, and used as needed by the board.
The software tool leads you step for step through the calibration process. For details of the DLL function see the **PD24222 driver manual**.

## 7 Register assignment:

**Channel A**

| ADDRESS | OPERATION | DATA | DESCRIPTION |
|---|---|---|---|
| 00 Hex | W | 0000 - FFFF Hex | Write level compare trigger value. Bit 0 to 15 compared to ADC bit 24 to 8 |
| 01 Hex | R and W | 00000 - FFFFF Hex | Read or write address counter |
| 02 Hex | R and W | 0000 - FFFFFF (auto increment) | Read or write to memory |
| 03 Hex | W | 0 - F Hex | Write capture divider |
| 04 Hex | W | 00 Hex Front trigger<br>01 Hex PXI trigger 0<br>02 Hex PXI trigger 1<br>03 Hex PXI trigger 2<br>04 Hex PXI trigger 3<br>05 Hex PXI trigger 4<br>06 Hex PXI trigger 5<br>07 Hex PXI trigger 6<br>08 Hex PXI trigger 7<br>09 Hex PXI STAR trigger<br>0A<br>0B<br>10 Hex Software trigger on<br>11 Hex Software trigger on | Select Trigger source |
| 05 Hex | W | 00 Hex positive level triggering<br>01 Hex negative level triggering<br>02 Hex positive edge triggering<br>03 Hex negative edge triggering<br>04 Hex positive edge, continuous triggering<br>05 Hex negative edge, continuous triggering | Select trigger edge |
| 06 Hex or 86 Hex | W | 0 - F Hex | Write clock source divider (same for A and B) |
| 06 Hex or 86 Hex | W | 10 Hex is divide by 2 for 50 : 50 duty cycle | Enable 50 : 50 duty cycle. ( clock source divider ratio divide by 2) |
| 07 Hex or 87 Hex | W | 00 Hex Clock 1 - 45.1584MHz<br>04 Hex Clock 2 - 73.728MHz<br>01 Front clock input<br>02 CLK from 24 bit AWG<br>03 PXI clock 10 MHz | Write clock source selector<br>(Combine with Clock divider) |
| 08 Hex | W | 1 Hex channel A loopmode enable | Write loopmode bit |
| 09 Hex or 89 Hex | W | (bit0=Do/Di bit1=CLK bit3=CS) | Read Write EEPROM |
| 0A Hex or 8A Hex | W | bit 0 = serial data input<br>bit 1 = Serial clock<br>bit 2 = Input offset channel A<br>bit 3 = Input offset channel B<br>bit 4 = Relay driver CS<br>bit 5 = ADC filter selector CS | Serial DATA bus<br>Serial CLOCK bus<br>Input offset CH-A Chipselect<br>Input offset CH-B Chipselect<br>Relay driver Chip select<br>ADC Sample Freq/ Filter select CS |
| 0B Hex or 8B Hex | W | xx Hex | ADC Reset. After reset an offset calibration from the ADC starts. Wait for (8704 x 1/Fs) (normal mode) after calibration start |
| 0F Hex | W | 00 Hex Unlock (bus access mode)<br>01 Hex Lock (capture mode, ready for trigger) | Lock on or off |

**Channel B**

| ADDRESS | OPERATION | DATA | DESCRIPTION |
|---|---|---|---|
| 80 Hex | W | 0000 - FFFF Hex | Write level compare trigger value. Bit 0 to 15 compared to ADC bit 24 to 8 |
| 81 Hex | R and W | 00000 - FFFFF Hex | Read or write address counter |
| 82 Hex | R and W | 0000 - FFFFFF (auto increment) | Read or write to memory |
| 83 Hex | W | 0 - F Hex | Write capture divider |
| 84 Hex | W | 00 Hex Front trigger<br>01 Hex PXI trigger 0<br>02 Hex PXI trigger 1<br>03 Hex PXI trigger 2<br>04 Hex PXI trigger 3<br>05 Hex PXI trigger 4<br>06 Hex PXI trigger 5<br>07 Hex PXI trigger 6<br>08 Hex PXI trigger 7<br>09 Hex PXI STAR trigger<br>0A<br>0B<br>10 Hex Software trigger on<br>11 Hex Software trigger on | Select Trigger source |
| 85 Hex | W | 00 Hex positive level triggering<br>01 Hex negative level triggering<br>02 Hex positive edge triggering<br>03 Hex negative edge triggering<br>04 Hex positive edge, continuous triggering<br>05 Hex negative edge, continuous triggering | Select trigger edge |
| 86 Hex or 06 Hex | W | 0 - F Hex | Write clock source divider same for A and B |
| 86 Hex or 06 Hex | W | 10 Hex is divide by 2 for 50 : 50 duty cycle | Enable 50 : 50 duty cycle. ( clock source divider ratio divide by 2) |
| 87 hex or 07 Hex | W | 00 Hex Clock 1 - 45.1584MHz<br>04 Hex Clock 2 - 73.728MHz<br>01 Front clock input<br>02 CLK from 24 bit AWG<br>03 PXI clock 10 MHz | Write clock source selector<br>(Combine with Clock divider) |
| 88 Hex | W | 1 Hex channel B loopmode enable | Write loopmode bit |
| 89 Hex or 09 Hex | W | (bit0=Do/Di bit1=CLK bit3=CS) | Read Write EEPROM |
| 8A Hex or 0A Hex | W | bit 0 = serial data input<br>bit 1 = Serial clock<br>bit 2 = Input offset channel A<br>bit 3 = Input offset channel B<br>bit 4 = Relay driver CS<br>bit 5 = ADC filter selector CS | Serial DATA bus<br>Serial CLCOK bus<br>Input offset CH-A Chipselect<br>Input offset CH-B Chipselect<br>Relay driver Chip select<br>ADC Sample Freq/ Filter select CS |
| 8B Hex or 0B Hex | W | xx Hex | ADC Reset. After reset an offset calibration from the ADC starts. Wait for (8704 x 1/Fs) (normal mode) after calibration start |
| 8F Hex or 0F Hex | W | 00 Hex Unlock (bus access mode)<br>01 Hex Lock (capture mode, ready for trigger) | Lock on or off |

### 7.1 Serial data bus commandos

**Channel A Relay driver serial data**

| Relay Driver (16 bits register) | |
|---|---|
| Data | Description |
| 3100 Hex | input -20dB |
| 3101 Hex | input -10dB |
| 3102 Hex | input 0dB |
| 3104 Hex | input +10dB |
| 3108 Hex | input +20dB |
| 3110 Hex | input +30dB |
| 3120 Hex | filter 22khz |
| 3140 Hex | filter 100khz |
| | |
| 2101 Hex | connect A+ input |
| 2102 Hex | connect A- input |
| 2104 Hex | DC coupling |
| 2108 Hex | 600R impedance |
| 2110 Hex | input offset |

| ADC settings (8 bits register) | |
|---|---|
| Data | Description |
| 00Hex | Sample Frequency = 48kHz |
| 01Hex | Sample Frequency = 96kHz |
| 02Hex | Sample Frequency = 192kHz |
| 04Hex | Enable 1Hz high pass filter |

**Channel B Relay driver serial data**

| Relay Driver (16 bits register) | |
|---|---|
| Data | Description |
| 0100 Hex | input -20dB |
| 0101 Hex | input -10dB |
| 0102 Hex | input 0dB |
| 0104 Hex | input +10dB |
| 0108 Hex | input +20dB |
| 0110 Hex | input +30dB |
| 0120 Hex | filter 22khz |
| 0140 Hex | filter 100khz |
| | |
| 1101 Hex | connect B+ input |
| 1102 Hex | connect B- input |
| 1104 Hex | DC coupling |
| 1108 Hex | 600R impedance |
| 1110 Hex | input offset |

| ADC settings (8 bits register) | |
|---|---|
| Data | Description |
| 00Hex | Sample Frequency = 48kHz |
| 01Hex | Sample Frequency = 96kHz |
| 02Hex | Sample Frequency = 192kHz |
| 04Hex | Enable 1Hz high pass filter |

# 8 Specifications:

**General:**

| | |
|---|---|
| Number of channels | 2 channel simultaneously sampled |
| ADC resolution | 24 bit |
| Converter type | Delta Sigma |
| Sample rate | 1kHz…220kHz |
| ADC oversampling modes | 64x 128x and 256x |
| Memory depth | 1M per channel |

**Analog:**

| | |
|---|---|
| Input configuration | Differential or single ended |
| Input impedance | 1MΩ / 600Ω software selectable |
| Input coupling | AC or DC software selectable |
| DC offset range | -5 Volt to +5Volt |
| Input filters | 22kHz or 100kHz Lowpass |

Input ranges

| Gain (dB) | voltage range |
|---|---|
| 0dB | 10Vpp |
| 10dB | 3.16Vpp |
| 20dB | 1Vpp |
| 30dB | 316mVpp |
| 40dB | 100mVpp |
| 50dB | 31.6mVpp |

**Dynamic characteristics:**

| | |
|---|---|
| Frequency response | 0.2dB from 20Hz to 20kHz |
| Absolute accuracy | +/- 0.05 dB @ 1kHz 10Vpp |
| SFDR (fs = 192kHz / Vin = 10Vpp) | 110 dB |
| THD (fs = 192kHz / Vin = 10Vpp) | 105 dB |
| SINAD (fs = 192kHz / Vin = 10Vpp) | 103 dB |

**Sample clock:**

| | |
|---|---|
| Clock sources | SMB front, internal crystal oscillator, PXI bus |
| Internal clock frequencies | 45.1584 MHz / 73.728 MHz |
| External clock frequency range | 64kHz…100MHz |
| External clock levels | Vlow < 0.6V Vhigh > 1.4Volt |
| External clock impedance | 50Ω DC |

**Triggering:**

| | |
|---|---|
| Trigger sources | Front, PXI trigger 0…7, PXI star trigger, software trigger, analog trigger |
| Trigger modes | Positive level, negative level, positive edge, negative edge, positive edge continuous and negative edge continuous |
| Front trigger impedance | 10kΩ DC |
| Front trigger levels | Vlow < 0.6V Vhigh > 2.4Volt |

**Power Requirements:**

maximum power consumtion

| +3.3 Volt | +5 Volt | +12 Volt | -12 Volt |
|---|---|---|---|
| | | | |

**Environment:**

| | |
|---|---|
| Operating temperature | 0 to 50°C |
| Storage temperature | 0 to 70°C |
| Relative humidity | 10 to 80 %, non-condensing |

**Mechanical**

| | |
|---|---|
| Size | single slot, 3U high |
| Weight | 210 gram |

# 9 Dynamic performance

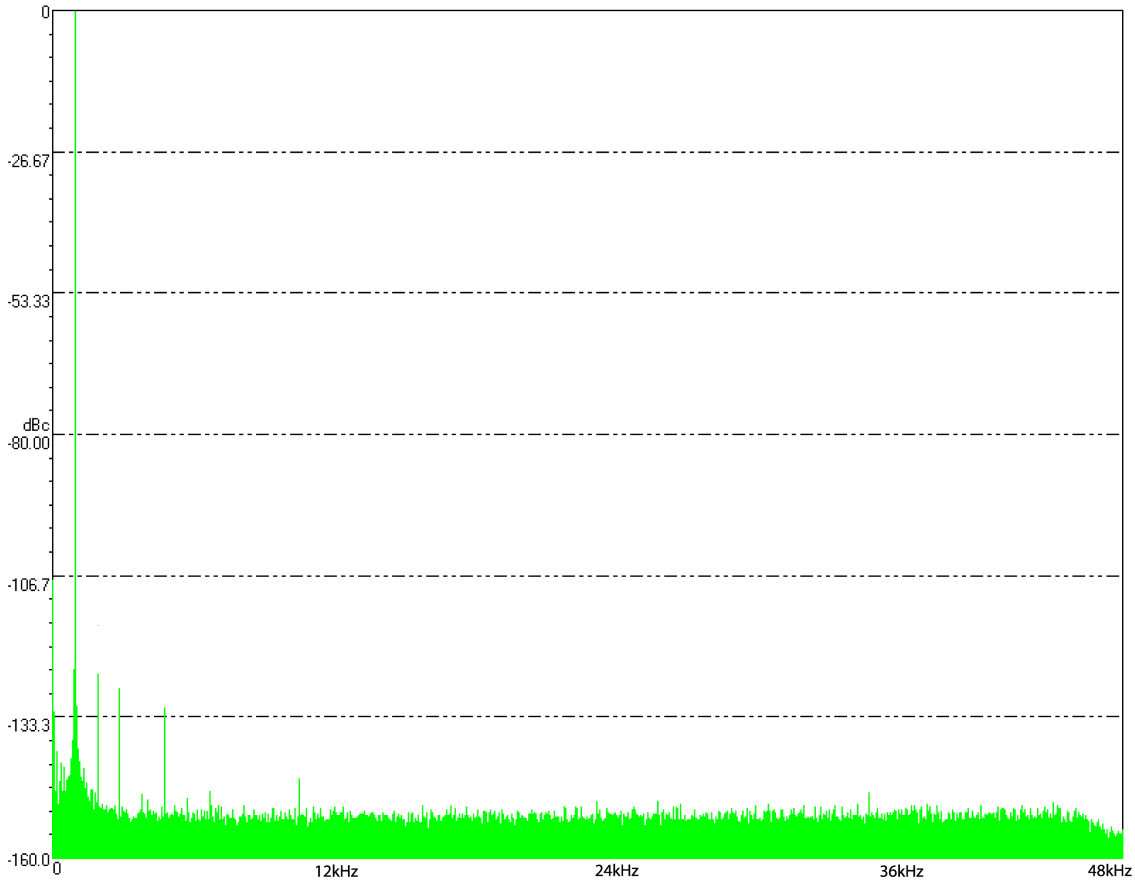


**Figure 9 Dynamic performance with 1kHz input signal**