GX5296

Digital I/O PXI Board

User's Guide

Last Updated Monday, August 10, 2016

MARVIN TEST SOLUTIONS

Safety and Handling

Each product shipped by Marvin Test Solutions is carefully inspected and tested prior to shipping. The shipping box provides protection during shipment, and can be used for storage of both the hardware and the software when they are not in use.

The circuit boards are extremely delicate and require care in handling and installation. Do not remove the boards from their protective plastic coverings or from the shipping box until you are ready to install the boards into your computer.

If a board is removed from the computer for any reason, be sure to store it in its original shipping box. Do not store boards on top of workbenches or other areas where they might be susceptible to damage or exposure to strong electromagnetic or electrostatic fields. Store circuit boards in protective anti-electrostatic wrapping and away from electromagnetic fields.

Be sure to make a single copy of the software CD for installation. Store the original CD in a safe place away from electromagnetic or electrostatic fields. Return compact disks (CD) to their protective case or sleeve and store in the original shipping box or other suitable location.

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If You Need Help

Visit our web site at http://www.marvintest.com more information about Marvin Test Solutions products, services and support options. Our web site contains sections describing support options and application notes, as well as a download area for downloading patches, example, patches and new or revised instrument drivers. To submit a support issue including suggestion, bug report or questions please use the following link: http://www.marvintest.com/magic/

You can also use Marvin Test Solutions technical support phone line (949) 263-2222. This service is available between 8:30 AM and 5:30 PM Pacific Standard Time.

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Table of Contents

Chapter 1 - Introduction

Manual Scope and Organization

Manual Scope

The purpose of this manual is to provide all the necessary information to install, use, and maintain the GX5296 (referred in this manual as GX5296) digital subsystem. This manual assumes the reader has a general knowledge of PC based computers, Windows operating systems, and some understanding of digital I/O.

Refer to the GtDio6x for more information regarding the GtDio6x software including driver functions, programming examples, virtual panel and more.

Manual Organization

The **GX5296** manual is organized in the following manner:

Chapter	Content
Chapter 1 - Introduction	Introduces the this manual. Lists all the supported GX5296 boards and shows warning conventions used in the manual.
Chapter 2 – Overview	Describes the GX5296 series features, board description, architecture, specifications.
Chapter 3 –Installation and Connections	Provides instructions on how to install a GX5296 boards and the GtDio6x software.
Chapter 4 – Theory of Operation	Presents the theory of operation for the GX5296 boards, with an overview of operation and a simple description of operation for one channel (I/O pin).

Conventions Used in this Manual

Symbol Convention	Meaning
	Static Sensitive Electronic Devices. Handle Carefully.
	Warnings that may pose a personal danger to your health. For example, shock hazard.
	Cautions where computer components may be damaged if not handled carefully.
	Tips that aid you in your work.

Formatting Convention	Meaning
`Monospaced Text`	Examples of field syntax and programming samples.
Bold type	Words or characters you type as the manual instructs. For example: function or panel names.
Italic type	Specialized terms. Titles of other reference books. Placeholders for items you must supply, such as function parameters

Chapter 2 - Overview

Introduction

The GX5296 offers the most performance and features of any 3U PXI dynamic digital I/O board on the market today. The 32-channel, GX5296 offers timing per pin, multiple time sets, data formatting, and an advanced sequencer – providing users with the capability emulate and test complex digital busses for system, board or device test applications. Offering 1 ns edge placement resolution per pin and a PMU per pin, the GX5296 has the ability to perform both DC and AC parametric testing. Each digital channel can be individually programmed for a drive hi, drive lo, sense hi, sense lo, and load value (with commutation voltage level). In addition, each channel offers a parametric measurement unit (PMU) providing users with the capability to perform parallel DC measurements on the DUT (device under test).

The GX5296 supports deep pattern memory by offering 64 Mb per pin of vector memory with dynamic per pin direction control and with test rates up to 125 MHz. The board supports both Stimulus / Response and Real-time Compare modes of operation, allowing the user to maximize test throughput for go / no-go testing of components and UUTs that require deep memory test patterns. The single board design supports both master and slave functionality without the use of add-on modules.

Features

The GX5296's timing generator supports 4 timing phases and windows (drive and sense timing). Each phase and window is comprised of two timing edges - assert / de-assert and an open window / close window respectively. Timing resolution of 1ns is supported for each of these edges. Four Timing sets are available for mapping edge timing to each channel. Up to 64 unique time set combinations can be defined. Additionally, six data formats are supported - NR (no return), R0, R1, RHiZ, and RC (Return to Complement), RSC (Return Surround with Complement).

Pin electronic resources are independent on a per channel basis and include a full-featured PMU for DC characterization of DUTs. The PMU can operate in the force voltage / measure current or force current / measure voltage mode. Additionally, 4 additional pin electronics resources are available for use as timing and/or control resources – providing programmable drive and sense levels from -2 to +7 volts.

The GX5296 employs a PLL based, clock system which offers programmable vector clock rates up to 125 MHz. In addition, a Clocks per Vector(CPV) divider is available, providing additional clocking and edge placement flexibility. External input and output synchronization signals are also supported, providing the ability to synchronize the GX5296 to external events or time bases.

The GX5296's offers a full-featured sequencer. Capabilities include conditional jump, unconditional jump, subroutine jump, or looping (with up to 16 nested loops). Additionally, the sequencer has the ability to handshake with various signals in order to synchronize with a UUT. Handshaking settings can be selected on a per Step basis where various Handshake Pause and Resume resources can be used. Total sequencer memory size is 4096 steps.

The following provide a summary of the GX5296 series main features:

- Cycle based, 125 MHz dynamic digital subsystem with high performance timing generator
- Pin electronics with per channel programmability
- Per channel parametric measurement unit (PMU)
- Per channel Dual level drive / sense, and programmable active load.
- 64 timing sets, each with 4 phases and 4 windows.
- 0 - 64 us phase and window programming range with 1ns resolution
- Supports up to 528 bi-directional I/O channels
- 64M of vector memory

- 3U PXI Instrument

PXI Compatibility

The GX5296 subsystem can operate in any 3U/6U PXI chassis that supports an air flow rate of 20 cfm/slot. The GX5296 subsystem can be used with a Marvin Test Solutions GX7305A / GX7015A PXI chassis which is designed specifically for high performance / high power digital applications and includes the necessary pin electronics power supplies as well as a high capacity cooling system.

Software

The GX5296 series is supplied with the GtDio6x software package that includes vector editing, a virtual instrument panel, and 32/64-bit DLL driver libraries and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, LabView, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, and Pascal. On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.

Other optional software packages are available to support the importing of legacy digital test programs, CASS digital TPS'a or IEEE-1445 .tap files.

Refer to the GtDio6x for more information regarding the GtDio6x software including driver functions, programming examples, virtual panel and more.

Applications

The GX5296 digital subsystem can be used to support a variety of digital test applications including:

- Semiconductor test
- ASICs testing
- A/D and D/A testing
- Video acquisition / playback applications
- High speed, bi-directional bus testing / emulation

Boards Description

The GX5296 has 2 connectors, J1 (I/O) and J3 (Auxiliary I/O) on the front and 1 PXI on the back

Figure 2-1: GX5296 Board

GX5296 Models and Accessories

Model / Accessory	Description
GX5296, DIO board	Digital input/output and domain timing and control.
GT95014, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface, Aux channels
GT95015, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Differential	
GT95015- SCSI, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Differential, no J2 connector installed	
Connector I/F for GX5296, SCSI to 100 Mil Grid, Single Ended (both 64 & 14 pin)	
GT95021, 2' shielded cable for GX5296 (68 Pin)	
GT95022, 3' shielded cable for GX5296 (68 Pin)	
GT95031, 6' shielded cable for GX5296 (68 Pin)	
GT95028,10' shielded cable for GX5296 (68 Pin)	

GX5296 Specifications

The following table outlines the specifications of the GX5296 board.

Channel I/O Specifications	
Number of Data I/O Channels	32 per card
Auxiliary I/O Channels	4, can be used for timing / control functions. Auxiliary channels offer all features supported by the data channels including a PMU per channel without vector memory.
Channel Direction Control	Input or Output per vector, per channel
Number of Drive and Sense Voltage References	32 Drive Hi / Drive Lo 32 Sense Hi / Sense Lo
Drive Voltage Level	Drive Hi: -2 V to +7 V Drive Lo: -2 V to +7 V Maximum swing: 8 V
Drive Voltage Accuracy	±15 mV (max)
Drive Voltage Resolution	16 bits, 250 uV
Driver Leakage Current	±15 nA (max)
Output Impedance	50 Ω (typ)
Drive Current	±35 mA (max)
Rise / Fall Times	0.5 ns typical for a 2 V pulse
Channel Skew	160 ps, typical between the same card 320 ps max, after calibration, for all channels within a domain (Drive and sense)
Sense Voltage Range	Sense Hi: -2 V to +7 V Sense Lo: -2 V to +7 V
Sense Voltage Threshold Accuracy	±15 mV
Sense Voltage Resolution	16 bits, 250 uV
Input Leakage Current	±15 nA (max)
Minimum Data Sense Pulse Width	1.0 ns (typ)
Pull-Up / Pull-Down Current Source / Sink	±24 mA, programmable on a per channel basis V commutate: -2 V to +7 V, programmable on a per channel basis
Pull-Up / Pull-Down Current Source / Sink Accuracy	±64 uA
Pull-Up / Pull-Down Current Source / Sink Resolution	16 bits
Voltage Commutation Accuracy	±15 mV
Voltage Commutation Resolution	16 bits
Memory	64 Mb per channel
Data Output Formats (per channel)	Drive Hi, Drive Lo, Hi-Z Formatted Data: No return, Return to 1, Return to 0, Return to Hi-Z, Return to complement, Surround by complement; selectable on a per channel basis
Drive Data Timing (per channel)	Data assert / de-assert based on Phases 0-3 (Firmware 0xAA03)

	Data assert / de-assert based on Phases 0-7 (Firmware 0xAA04 and above)
Capture Mode (per channel)	Mask Opening edge of Window Closing edge of Window Window – data is valid for entire window duration
Test Modes	
Drive / Expect Mode	Output: Drive Hi, Drive Lo, Hi-Z Expect: 1, 0, OK, between states, or mask Keep last Toggle last
Recording Modes (per sequence step)	Record errors for programmable inputs that have Good 1 & Good 0 Record errors for inputs that have only a Good 1 Record raw data based on NOT a Good 0 Record raw data based on a Good 1
Error Address Record	Record address for memory errors 1K deep error memory
Timing	
Master Clock (PLL) Frequency Range	1 MHz (min); 125 MHz (max)
Programming Resolution	5 digits
Accuracy	±0.02% of programmed value + accuracy of reference clock (PXI 10 MHz or external reference clock)
Jitter	50 ps RMS, typical
Reference	PXI 10 MHz clock or XClk (external clock) input
Clocks per Vector Range	Programmable, 1 to 64
Time Sets	Firmware 0xAA03: 4 phases, 4 windows, user assigned to DIO channels Firmware 0xAA04 (and above): 8 phases, 4 windows, user assigned to DIO channels
Timing Set Sequence Control	Firmware 0xAA03: 64 Timing Sets with 4 Phases, 4 Windows, and 4 K sequence steps. Firmware 0xAA04 (and above): 64 Timing Sets with 8 Phases, 4 Windows, and 4 K sequence steps.
Phase and Window Timing Resolution	1 ns, using the 125 MHz master clock
Minimum Phase / Window Pulse Width; Assert / Return Or Open / Close	5 ns
Phase / Window Reference	Phase: System or Pattern Clock (selectable per Seq Step) Window: Pattern clock only
External Status and Control Signals	
Logic Levels	LVTTL or programmable level using one of the four Aux pin electronics channels.
Trigger Source	Software, PXI trigger bus, External event, External trigger input

Sync Outputs	Start of Sequence; Start of Sequence Step
Input Aux I/O Selections	Synthesizer reference clock, System clock, Break (System Clutch), Halt (Pattern Clutch), Sequence Jump signals
Output Aux I/O Selections	Phase, Window, Waveform, Syncs, Seqflag, Seq Active, Seq Idle, T0_Clk , Pat_Clk,
Sequencer	
Commands	Jump, Conditional Jump, Loop, Call Subroutine, Return, Pause, Halt
Loop Counters	16, can be nested Only one can end on a sequence step Loop count range: 1 – 64K or continuous
Test Inputs	External: PXI triggers, Aux I/O Internal: Data sense, Edge or level
Sequencer Memory	4096 Steps
Phase Trigger	T0_CLK (Sytem Clock) or PAT_CLK (Vector clock)
Window Trigger	PAT_CLK (Vector clock)
Patterns per Sequence Step	1 to 64M
Sequence Loop	1 to 1M, continuous
Current Step Loop	1-65535, continuous
Multi Step Loop	1-65535, nested 16 deep
Jump	Conditional / Unconditional
Jump Conditions	Error True, Sequence Timeout True, Signal Level (High / Low), Signal Edge (Rising / Falling)
Parametric Measurement (PMU)	
Number of Parametric Measurement Units	32, one per channel 4, one per auxiliary channel (for timing /control & static I/O functions)
Configurations	Force Voltage/Measure Current (FVMI) Force Current/Measure Voltage (FIMV) Force Voltage/Measure Voltage (FVMV) Force Current/Measure Current (FIMI)
Force Voltage Range	-1.5 V to +7 V
Force Voltage Accuracy	±15 mV
Force Voltage Resolution	16 bits
Force Current Ranges	±32 mA, ±8 mA, ±2 mA, ±512 uA, ±128 uA, ±32 uA, ±8 uA, ±2 uA FS
Force Current Accuracy; Compliance Range: +7 V to +1.75 V @ 32 mA, +7 V to -1.5 V @ no load	±120 uA, 32 mA range ±40 uA, 8 mA range ±5uA, 2 mA range ±1.2 uA, 512 uA range ±600 nA, 128 uA range ±160 nA, 32 uA range ±80 nA, 8 uA range ±20 nA, 2 uA range

Current Measurement Accuracy (60 Measurements / Sec); Compliance Range: +7 V to +1.75 V @ 32 mA +7 V to -1.5 V @ no load	±120 uA, 32 mA range ±40 uA, 8 mA range ±5 uA, 2 mA range ±1.2 uA, 512 uA range ±600 nA, 128 uA range ±160 nA, 32 uA range ±80 nA, 8 uA range ±20 nA, 2 uA range
Measure Voltage Range	-2 V to +7 V
Measure Voltage Accuracy	±1 mV (measurement rate < 200 measurements / sec)
High and Low Commutation Voltage Range	VCLo: -2 V to +5 V VCHi: 0 V to +7 V
Voltage Clamp Accuracy	±100 mV
Power (Idle and Initialized)	
+3.3 VDC	4.8 A
+5 VDC	1.48 A
+12 VDC	0.25 A
Environmental	
Operating Temperature	0 °C to +50 °C
Storage Temperature	-20 °C to +70 °C
Size	3U PXI
Weight	200 g
Front Panel Connectors	
J1	Digital I/O Signals, type 68-pin VHD connector
J3	Timing & Control Signals, type 68-pin VHD connector

Chapter 3 - Installation and Connections

Getting Started

This section includes general hardware installation procedures for the GtDio6x board and installation instructions for the GtDio6x software. Before proceeding, please refer to the appropriate chapter to become familiar with the board being installed.

To Find Information on:	**Refer to:**
Hardware Installation	This Chapter
GtDio6x Driver Installation	This Chapter
Theory of Operation	Chapter 4

Interfaces and Accessories

The following accessories are available from Marvin Test Solutions the GX5296 series digital subsystem:

Part / Model Number	**Description**
GT95014, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface, Aux channels
GT95015, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Differential	
GT95015- SCSI, Connector Interface for the GX5296, SCSI to 100 Mil Grid, Differential, no J2 connector installed	
GT95021, 2' shielded cable for GX5296 (68 Pin)	
GT95022, 3' shielded cable for GX5296 (68 Pin)	
GT95031, 6' shielded cable for GX5296 (68 Pin)	
GT95028,10' shielded cable for GX5296 (68 Pin)	

Packing List

All GX5296 boards have the same basic packing list, which includes:

- GX5296 Board
- GtDio6x Software Disk

Unpacking and Inspection

After removing the board from the shipping carton:

 **Caution -** Static sensitive devices are present. Ground yourself to discharge static.

Remove the board from the static bag by handling only the metal portions.

Be sure to check the contents of the shipping carton to verify that all of the items found in it match the packing list.

Inspect the board for possible damage. If there is any sign of damage, return the board immediately. Please refer to the warranty information at the beginning of the manual.

System Requirements

The GX5296 PXI digital subsystem is designed to run on 6U PXI compatible chassis running under XP or newer (32/64 bit).

Each board in the digital subsystem requires one unoccupied 6U PXI bus slot.

Installation of the GtDio6X Software

Before installing the board it is recommended that you install the GtDio6x software as described in this section. To install the GtDio6x software, follow the instruction described below:

Insert the Marvin Test Solutions CD-ROM and locate the **GtDio6x.EXE** setup program. If you computer's Auto Run is configured, when inserting the CD a browser will show several options. Select the Marvin Test Solutions Files option and then locate the setup file. If Auto Run is not configured you can open the Windows explorer and locate the setup files (usually located under \Files\Setup folder). You can also check and see if a newer version of the software is available for download from Marvin Test Solutions' web site (www.marvintest.com), in that case download and use the newer version.

Run the GtDio6x setup and follow the instruction on the Setup screen to install the GtDio6x driver.

Note: When installing under Windows, you may be required to restart the setup after logging-in as a user with Administrator privileges. This is required in-order to upgrade your system with newer Windows components and to install kernel-mode device drivers (HW.SYS and HWDEVICE.SYS) which are required by the GtDio6x driver to access resources on your board.

The first setup screen to appear is the Welcome screen. Click **Next** to continue.

Enter the folder where GtDio6x is to be installed. Either click **Browse** to set up a new folder, or click **Next** to accept the default entry of `C:\Program Files\Marvin Test Solutions\GtDio6x` under 32-bit Windows or `C:\Program Files (x86)\Marvin Test Solutions\GtDio6x` under 64-bit Windows.

Select the type of Setup you wish and click **Next.** You can choose between **Typical**, **Run-Time** and **Custom** setups types. The **Typical** setup type installs all files. **Run-Time** setup type will install only the files required for controlling the board either from its driver or from its virtual panel. The **Custom** setup type lets you select from the available components.

The program will now start its installation. During the installation, Setup may upgrade some of the Windows shared components and files. The Setup may ask you to reboot after completion if some of the components it replaced were used by another application during the installation – do so before attempting to use the software.

You can now continue with the installation to install the board. After the board installation is complete you can test your installation by starting a panel program that lets you control the board interactively. The panel program can be started by selecting it from the Start, Programs, GtDio6x menu located in the Windows Taskbar.

Setup Maintenance Program

You can run the Setup again after GtDio6x has been installed from the original disk or from the Windows Control Panel – Add Remove Programs applet. Setup will be in the Maintenance mode when running for the second time. The Maintenance window show below allows you to modify the current GtDio6x installation. The following options are available in Maintenance mode:

- Modify. When you want to add or remove GtDio6x components.
- Repair. When you have corrupted files and need to reinstall.
- Remove. When you want to completely remove GtDio6x.

Select one of the options and click **Next** and follow the instruction on the screen until Setup is complete.

Overview of the GtDio6x Software

Once the software is installed, the following tools and software components are available:

- **GtDio6x Panel** – Configures and controls the GtDio6x board various features via an interactive user interface.
- **GtDio6x driver** - A DLL based function library (GTDIO6X.DLL for 32-bit applications or GTDIO6X64.DLL for 64-bit applications , located in the Windows System folder) used to program and control the board. The driver uses Marvin Test Solutions' HW driver or VISA supplied by third party vendor to access and control the GtDio6x boards.
- **Programming files and examples** – Interface files and libraries for support of various programming tools. A complete list of files and development tools supported by the driver is included in subsequent sections of this manual.
- **Documentation** – On-Line help and User's Guide for the board, GtDio6x driver and panel.
- **HW driver and PXI/PCI Explorer applet** – HW driver allows the GtDio6x driver to access and program the supported boards. The explorer applet configures the PXI chassis, controllers and devices. This is required for accurate identification of your PXI instruments later on when installed in your system. The applet configuration is saved to PXISYS.ini and PXIeSYS.ini and is used by Marvin Test Solutions instruments HW driver. The applet can be used to assign chassis numbers, Legacy Slot numbers and instrument alias names. The HW driver is installed and shared with all Marvin Test Solutions products to support accessing the PC resources. Similar to HW driver, provides a standard way for instrument manufacturers and users to write and use instruments drivers. VISA is a standard maintained by the VXI Plug & Play System Alliance and the PXI Systems Alliance organizations (http://www.vxipnp.org/, http://www.pxisa.org/). The VISA resource manager such as National Instruments **Measurement & Automation** (NI-MAX) displays and configures instruments and their address (similar to Marvin Test Solutions' PXI/PCI Explorer). The GtDio6x driver can work with either HW or VISA to control an access the supported boards.

Installation Folders

The GtDio6x driver files are installed in the default folder `C C:\Program Files\Marvin Test Solutions\GtDio6x` under 32-bit Windows or `C:\Program Files (x86)\Marvin Test Solutions\GtDio6x` under 64-bit Windows. During the installation, GtDio6x Setup creates and copies files to the following folders:

Name	Purpose / Contents
…\Marvin Test Solutions\GtDio6x	The GtDio6x folder. Contains panel programs, programming libraries, interface files and examples, on-line help files and other documentation.
…\Marvin Test Solutions\HW	HW device driver. Provide access to your board hardware resources such as memory, IO ports and PCI board configuration. See the README.TXT located in this directory for more information.
…\ATEasy\Drivers	ATEasy drivers folder. GtDio6x Driver and example are copied to this directory only if ATEasy is installed to your machine.
Windows System Folders	Contains the GtDio6x DLL and GtDio6x64.DLLdriver, HW driver shared files and some upgraded system components, such as the HTML help viewer, etc.

Configuring Your PXI System using the PXI/PCI Explorer

To configure your PXI/PCI system using the **PXI/PCI Explorer** applet follow these steps:

Start the PXI/PCI Explorer applet. The applet can be start from the Windows Control Panel or from the Windows Start Menu, **Marvin Test Solutions**, **HW**, **PXI/PCI Explorer**.

Identify Chassis and Controllers. After the PXI/PCI Explorer is started, it will scan your system for changes and will display the current configuration. The PXI/PCI Explorer automatically detects systems that have Marvin Test Solutions controllers and chassis. In addition, the applet detects PXI-MXI-3/4 extenders in your system (manufactured by National Instruments). If your chassis is not shown in the explorer main window, use the Identify Chassis/Controller commands to identify your system. Chassis and Controller manufacturers should provide INI and driver files for their chassis and controllers which are used by these commands.

Change chassis numbers, PXI devices Legacy Slot numbering and PXI devices Alias names. These are optional steps and can be performed if you would like your chassis to have different numbers. Legacy slots numbers are used by older Marvin Test Solutions driver. Alias names can provide a way to address a PXI device using a logical name (e.g. "FPGA1"). For more information regarding slot numbers and alias names, see the **GtDio6xInitialize** function.

Save your work. PXI Explorer saves the configuration to the following files located in the Windows folder: PXISYS.ini, PXIeSYS.ini and GxPxiSys.ini. Click on the **Save** button to save your changes. The PXI/Explorer will prompt you to save the changes if changes were made or detected (an asterisk sign ' *' in the caption indicated changes).

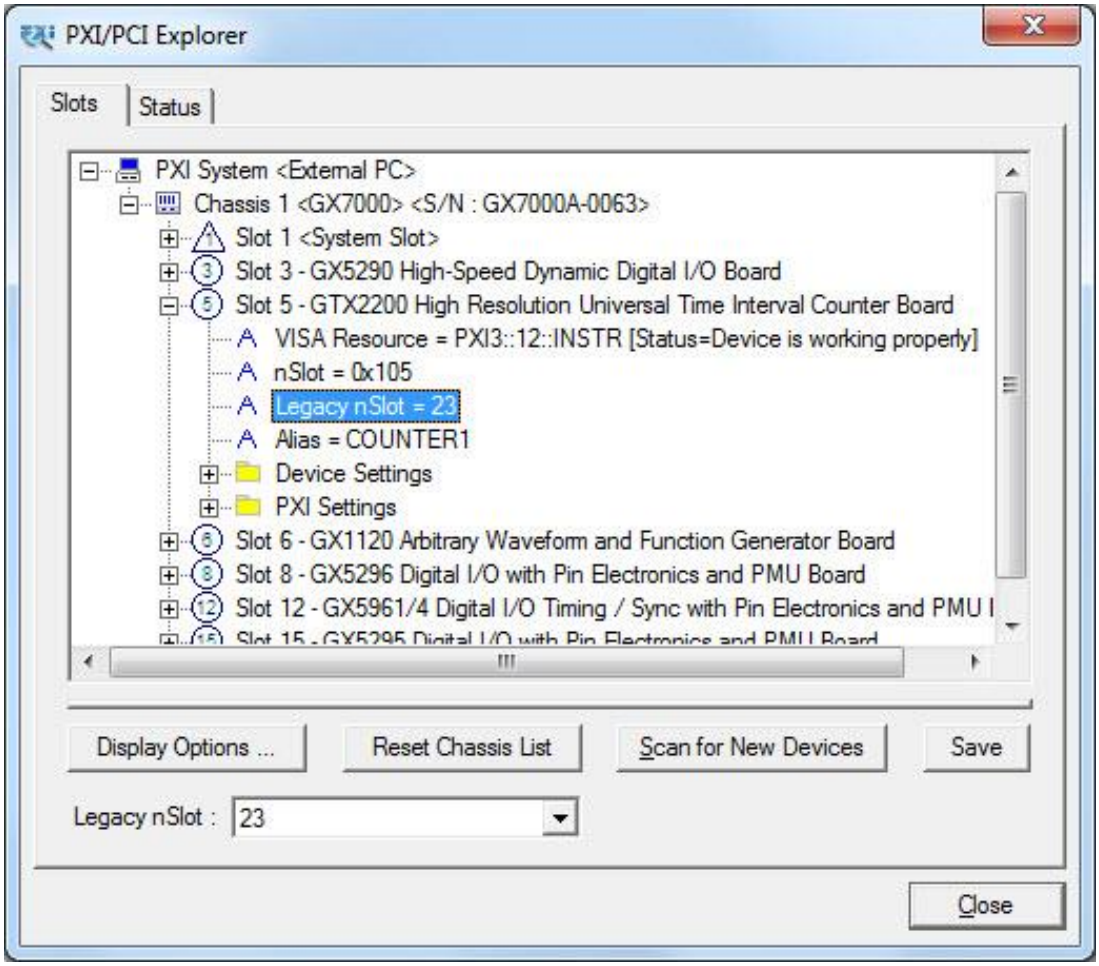

Figure 3-1: PXI/PCI Explorer

Board Installation

Before you Begin

- Install the GtDio6x driver as described in the prior section.
- Configure your PXI/PC system using **PXI/PCI Explorer** as described in the prior section.
- Verify that all the components listed in the packing list (see previous section in this chapter) are present.

Electric Static Discharge (ESD) Precautions

To reduce the risk of damage to the GX5296 board, the following precautions should be observed:

- Leave the board in the anti-static bags until installation requires removal. The anti-static bag protects the board from harmful static electricity.
- Save the anti-static bag in case the board is removed from the computer in the future.
- Carefully unpack and install the board. Do not drop or handle the board roughly.
- Handle the board by the edges. Avoid contact with any components on the circuit board.

Caution – Do not insert or remove any board while the computer is on. Turn off the power from the PXI chassis before installation.

Installing a Board

Install each of the boards as follows:

1. Install the GtDio6x software as described in the next section.
2. Turn off the PXI chassis and unplug the power cord.
3. Locate a PXI empty slot on the PXI chassis.
4. Place the module edges into the PXI chassis rails (top and bottom).
5. Carefully slide the PXI board to the rear of the chassis, make sure that the ejector handles are pushed out (as shown in Figure 3-2).

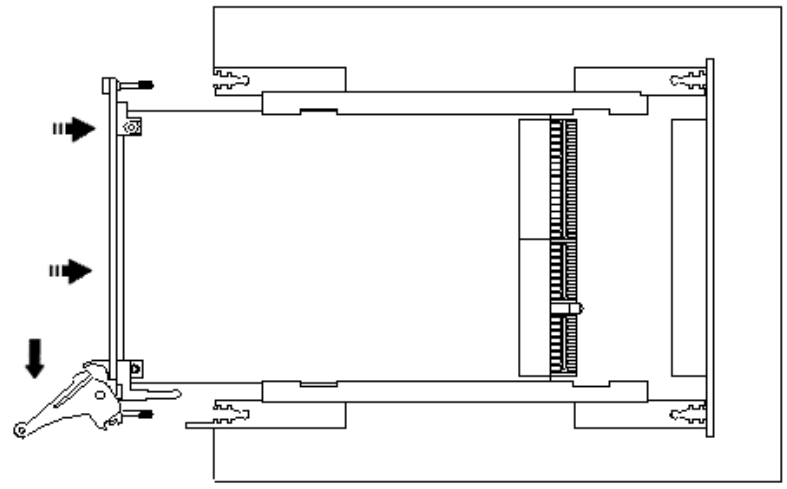

Figure 3-2: Ejector handles position during module insertion

6. After you feel resistance, push in the ejector handles as shown in Figure 3-3 to secure the module into the frame.

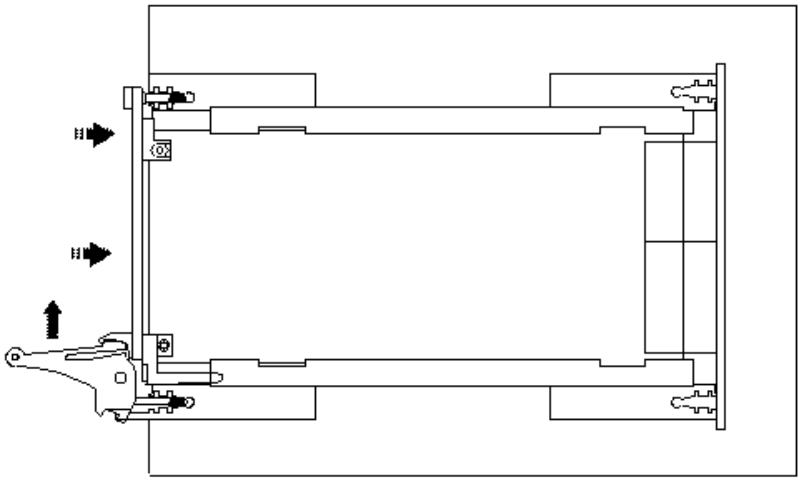

Figure 3-3: Ejector handles position after module insertion

7. Tighten the module's front panel to the chassis to secure the module in.
8. Connect any necessary cables to the board.
9. Plug the power cord in and turn on the PXI chassis.

Plug & Play Driver Installation

Plug & Play operating systems such as Windows 9x, Me, Windows 2000, XP, VISTA or Windows 7 (Not Windows NT) notifies the user that a new board was found using the **New Hardware Found** wizard after restarting the system with the new board.

If another Marvin Test Solutions board software package was already installed, Windows will suggest using the driver information file: HW.INF. The file is located in your Program Files\Marvin Test Solutions\HW folder. Click **Next** to confirm and follow the instructions on the screen to complete the driver installation.

If the operating system was unable to find the driver (since the GtDio6x driver was not installed prior to the board installation), you may install the GTDIO6X driver as described in the prior section, then click on the **Have Disk** button and browse to select the HW.INF file located in C:\Program File\Marvin Test Solutions\HW.

If you are unable to locate the driver click **Cancel** to the found New Hardware wizard and exit the New Hardware Found Wizard, install the GtDio6x driver, reboot your computer and repeat this procedure.

The Windows Device Manager (open from the System applet from the Windows Control Panel) must display the proper board name before continuing to use the board software (no Yellow warning icon shown next to device). If the device is displayed with an error you can select it and press delete and then press F5 to rescan the system again and to start the New Hardware Found wizard.

Removing a Board

Remove the board as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI slot on the PXI chassis.
3. Disconnect and remove any cables/connectors connected to the board.
4. Un-tighten the module's front panel screws to the chassis.
5. Push out the ejector handles and slide the PXI board away from the chassis.
6. Optionally – uninstall the GtDio6x driver.

Connectors and Jumpers

Figure 3-4 shows the available GX5964 and GX5961 board connectors:

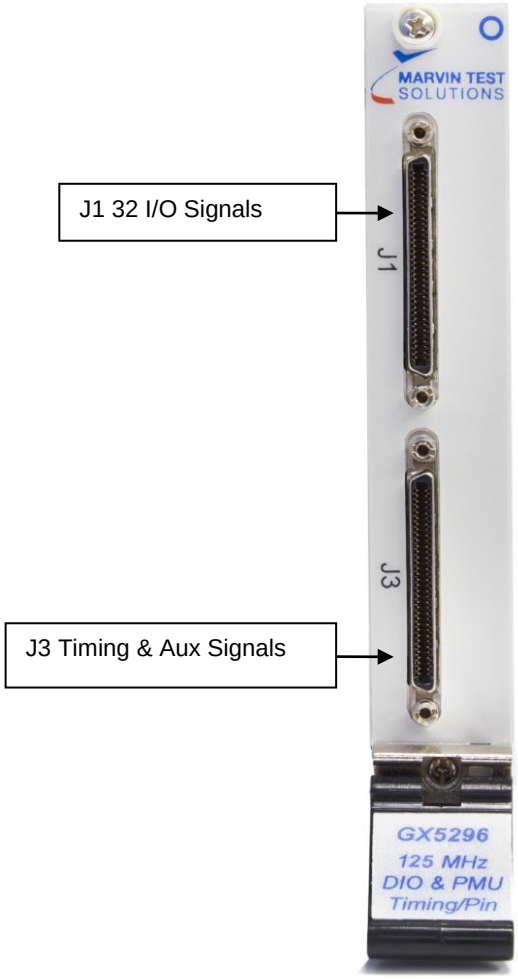

Figure 3-4: GX5296 Front Panel Connectors

The GX5296 has 2 connectors. All the connectors are available on the instrument's front panel. The GX5296 has the following connectors:

J1 I/O Signals - 68-pin VHD	Programmable I/O Levels Data Connector Signals.
J3 Timing - 68-pin VHD	Timing & Aux Signals (do not use timing signals on Slave boards).

J1 I/O Signals (68-Pin to UUT)

The following table defines the GX5296 DIO to I/O signals. This interface uses a 68-pin VHD connector.

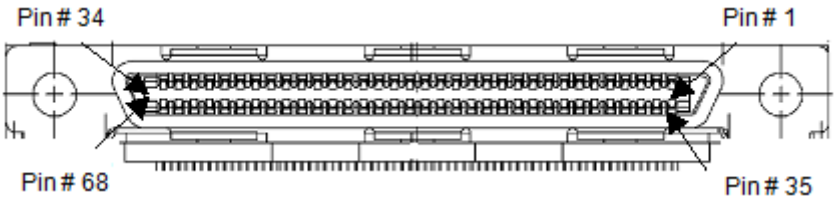

Figure 3-5: GX5296 Front Panel Connector 68 pin (VHD) connector

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	IO0	I/O	18	IO17	I/O	35	GND	GND	52	GND	GND
2	IO1	I/O	19	IO18	I/O	36	GND	GND	53	GND	GND
3	IO2	I/O	20	IO19	I/O	37	GND	GND	54	GND	GND
4	IO3	I/O	21	IO20	I/O	38	GND	GND	55	GND	GND
5	IO4	I/O	22	IO21	I/O	39	GND	GND	56	GND	GND
6	IO5	I/O	23	IO22	I/O	40	GND	GND	57	GND	GND
7	IO6	I/O	24	IO23	I/O	41	GND	GND	58	GND	GND
8	IO7	I/O	25	IO24	I/O	42	GND	GND	59	GND	GND
9	IO8	I/O	26	IO25	I/O	43	GND	GND	60	GND	GND
10	IO9	I/O	27	IO26	I/O	44	GND	GND	61	GND	GND
11	IO10	I/O	28	IO27	I/O	45	GND	GND	62	GND	GND
12	IO11	I/O	29	IO28	I/O	46	GND	GND	63	GND	GND
13	IO12	I/O	30	IO29	I/O	47	GND	GND	64	GND	GND
14	IO13	I/O	31	IO30	I/O	48	GND	GND	65	GND	GND
15	IO14	I/O	32	IO31	I/O	49	GND	GND	66	GND	GND
16	IO15	I/O	33	NC		50	GND	GND	67	NC	
17	IO16	I/O	34	DUT GND	GND	51	GND	GND	68	DUT GND	GND

Table B-6: J1 68-Pin I/O Signals

Notes:

- I/O0 – I/O31: Single Ended Data Lines.
- DUT GND – Device Under Test ground sense Input

J3 Timing Signals Connector

This section describes the GX5296 J3 Timing connector and external event signals (used only on a Master). This interface uses a 68-pin VHD connector. The following table lists the Timing signals:

Pin	Name	Function	Type
1-7	EXT0- EXT6	Reserved (not used)	I
8	NC	No Connection	
9	Auxiliary Channel 0/ Probe Signal	PMU/Input/Output/Probe Signal	I/O
10	Auxiliary Channel 1	PMU/Input/Output Functions	I/O
11	Auxiliary Channel 2	PMU/Input/Output Functions	I/O
12	Auxiliary Channel 3	PMU/Input/Output Functions	I/O
13	XMeasure	Ext-Measurement (Not To be used)	I
14-16	NC	No Connection	
17	Auxiliary Channel 4	TTL Output	O
18	Auxiliary Channel 5 – TTL Output	TTL Output	O
19	NC	No Connection	
20	NC	No Connection	
21	NC	No Connection	
22	Auxiliary Channel 6	TTL Output	O
23	NC	No Connection	
24	Auxiliary Channel 7	TTL Output	O
25	NC	No Connection	
26	Auxiliary Channel 8	TTL Input	I
27	Auxiliary Channel 9	TTL Input	I
28	Auxiliary Channel 10	TTL Input	I
29	Auxiliary Channel 11	TTL Input	I
30	SV	Super Voltage Input (Requires Factory Configuration)	I
31	Auxiliary Channel GP	General Purpose TTL Input	I
32	Auxiliary Channel GP	General Purpose TTL Input	I
33	NC	No Connection	
34-64	GND	Ground	G

Table B-7: J3 68-Pin Timing / Aux Signals

Notes:

1. Output functions that can be routed to any of the Aux channels via the API GtDio6xChannelSetAuxiliaryOutputSignal:
   - Waveforms 0 to 3
   - Sync pulse 0 & 1
   - Idle active
   - Burst active
   - Step flag 0
   - Step flag 1
   - Step clock
   - Vector clock
   - Raw error
   - T0 CLK
   - Sequence Clock
   - Pulse generator
   - Record active status
   - Jump strobe
   - Counter active
   - Vector clocks per vector DONE
   - Last Word
   - Burst count done
   - Loop count done
   - Gosub Active
   - Counted loop
   - Subroutine return
   - Return flag
   - Last sequence
2. Input functions that can be routed to the Aux channels:
   - Sequence clock
   - Jump
   - Jump strobe
   - Load sequence register
   - Load loop counter
   - Jump trigger (0 – 3)
   - PLL reference input
   - Vector clock input

Chapter 4 - Theory of Operation

This chapter presents the theory of operation for the GX5296 boards. The following points are discussed:

- Overview
- Architecture
- Sequencer Engine
- Master, System and Vector Clocks
- Timing Sets, Timing Modes and Timing Set Value rules
- Vector Memory
- Step Memory
- Record Memory
- Error Address Memory
- Test Logic
- I/O Channels

Overview

The GX5296 can run at frequencies up to 125 MHz with programmable timing sets applied on a per Step and Channel basis. Each board contains 32 I/O pins and each pin can be configured as an input or output on a per vector basis. Each board has up to 4K Steps and 64M Vectors. A Vector represents the drive, expect, mask, and Tri-State data for one state (one Vector clock cycle). The Vector states are represented as ASCII characters.

A Step is a higher level that includes clock, timing, and control settings as well as a pointer into the Vector Memory. Different Steps can have overlapping Vector ranges (Vector Count and Offset). Each Step contains timing set information that will be applied to the relevant Vectors.

The Timing Set consists of a Drive Phase Assert, and Return edge as well as a Capture Window Open and Close edge. The Phase edges determine when a Vector state will be loaded within a clock cycle. The Window edges determine when the input will be sampled within a clock cycle. Consequently, each channel has an associated capture mode that allows the sequencer to capture input on the Window open edge, close edge, throughout the entire Window or not at all.

The GX5296 includes one unified (Vector) memory, for storing drive, expect, mask, and Tri-State data for each of the 64M Vectors. A separate Record memory is used to store up to 64M response states (raw logic HI and LO) or real time error states (depending on a Step's record mode) recorded during a sequencer run.

One of the GX5296's functional modules is the sequencer. The GX5296 sequencer functions as a state machine with five main states: RUN, SOFT PAUSE, HARD PAUSE, IDLE, and RESET. The sequencer runs each Step sequentially, applying timing (phase and window) settings to the Vectors associated with the Step. The sequencer will also perform a conditional jump, unconditional jump, subroutine jump, or loop if so instructed by a Step.

The sequencer has the ability to Handshake with various signals in order to synchronize with a UUT. Handshaking settings can be selected on a per Step basis where various Handshake Pause and Resume resources can be used. Handhsake resources are configured for use by a Step. Configuring a Handshake resource entails selecting a source signal and test condition (high level, low level, rising edge, falling edge) to evaluate the source signal as a valid Pause or Resume condition.

Each digital pin can be individually programmed for a drive high, drive low, input threshold high, input threshold low, and a load value (with commutation voltage level). Each channel output can be formatted programmatically to one of the following formats: No Return, Return to Off (HiZ), Return to Zero, Return to One, Return to Complement, Surround Complement, Force Zero, Force One, Force Off (HiZ), Force inverse Phase Output, Force

Phase Output. Output formatting provides flexibility to create a variety of bus cycles and waveforms to test board and box level products. Each output channel can sense an over current sink or source condition, protecting each I/O channel from an overload condition. These conditions are recorded and the channel's output will go to a HI-Z state until the over current flag is cleared.

Each channel has its own Parametric Measurement Unit (PMU). The PMU offers the ability to perform analog measurements on each digital pin. Measurement configurations include force voltage, measure current and force current, measure voltage.

Additionally, under software control, each channel's operating temperature, Vcc / Vee voltage rails, drive high / drive low voltages, sense hi / sense lo voltages, and output current values can all be monitored and measured.

Each input channel's source and sink load currents can be set programmatically. The input channel current source forces the specified constant current to be active when the input voltage is above the high voltage clamp value. Each input channel's constant current voltage clamp can be set programmatically. With independent high and low clamping (commutating) voltages, the source and sink currents each have their own threshold voltage. Each input channel‘s load may be configured as a selectable resistor with pull-up and pull-down values or the value can be an open circuit. Each input channel's high and low voltage threshold comparator delays can be set programmatically.

Architecture

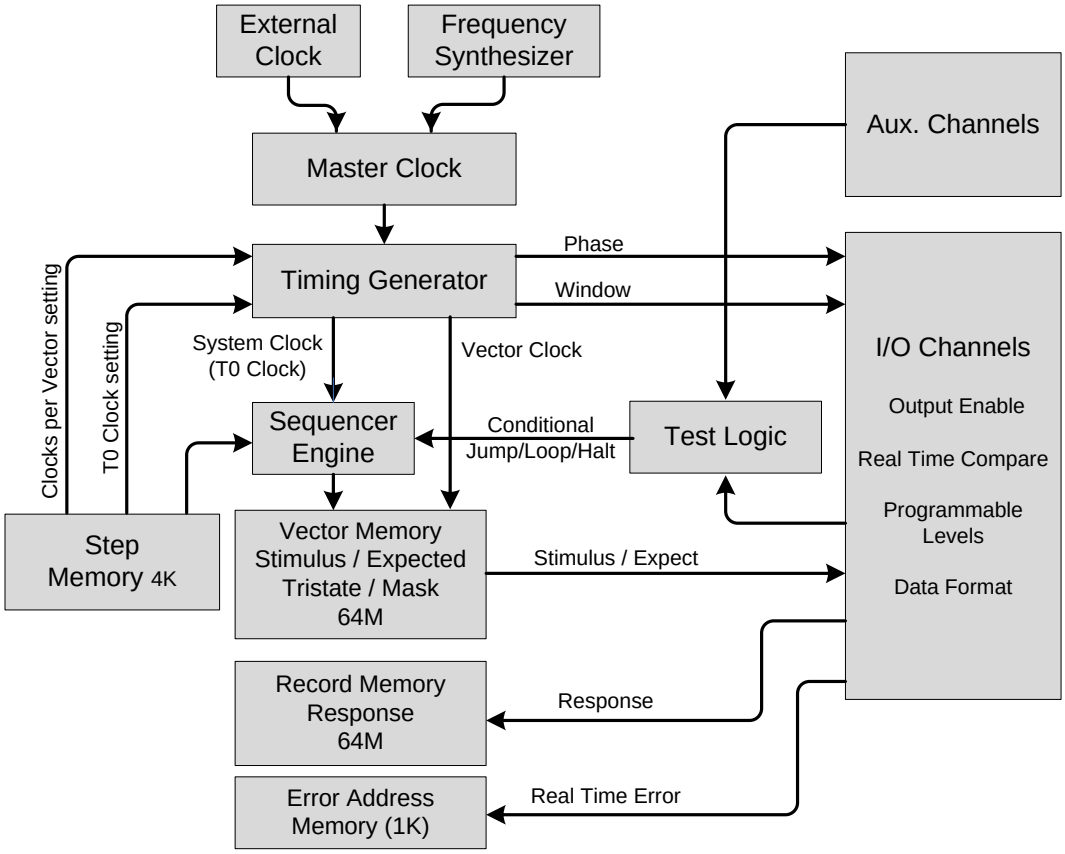

Figure 4-1: Architecture Block Diagram

Master Clock

The master clock functional block includes a Programmable Loop Lock Frequency Synthesizer. The reference clock for the Frequency Synthesizer can use the built-in 20 MHz oscillator, PXI Clock 10 MHz or an external oscillator in the range of 5 to 80 MHz.

Timing Generator

Using the Master Clock as a basis, the Timing Generator block produces a, Phase, Window, Vector and System clock signals. In a Master/Slave configuration, these signals are broadcast across the PXI Backplane (B/P) on the Local Bus signal lines to other board sequencers. The System clock is used by the sequencer to start each phase and window along with incrementing the Vector and Record memories. The System clock can be sourced from the internal T0 clock or an external source connected to an auxiliary channel.

Step Memory and Sequencer Engine

The Step Memory defines the order in which Vectors will be driven or sensed (recorded). This block provides the addressing to the Vector Memory and the Record Memory. The Step Memory also contains the T0 Clock period, Phase, Window, CPV (clocks per vector) and a Control statement for conditional jumping and looping

Vector Memory

The stimulus, expect, and Tri-State data for each vector and channel is stored in the Vector Memory.

Record Memory

The Record Memory stores individual channel error results or raw response data depending on the current Step's record mode.

Test Logic

The test logic monitors Auxiliary Channels, Error signal, Channel Compare signals, and PXI triggers and provides the Sequencer Engine with input for its conditional logic.

Aux I/O

The auxiliary I/O block offers a range of useful user and diagnostic input and output signals for user applications. The inputs may be used for synchronizing or triggering the GX5296 with UUT generated events.

I/O Channels

The channel I/O block takes the Stimulus data, applies the data format and outputs the formatted data according to the phase timing. The resultant Drive and Enable signals go to the Channel Drivers (pin electronics).

The Response High and Response Low signals from the Receivers are examined and based on the window timing and capture mode and the response is analyzed with respect to the Expect data. The cumulative Error signal goes to the Test Logic block so it can be used for Jumping, Halting and Counting of Errors.

Sequencer

The GX5296 board has six basic operational states: **Reset, Idle, Standby, Halt, Pause** and **Run**. Figure 4-2 is a block diagram showing the relationship of these operational states.

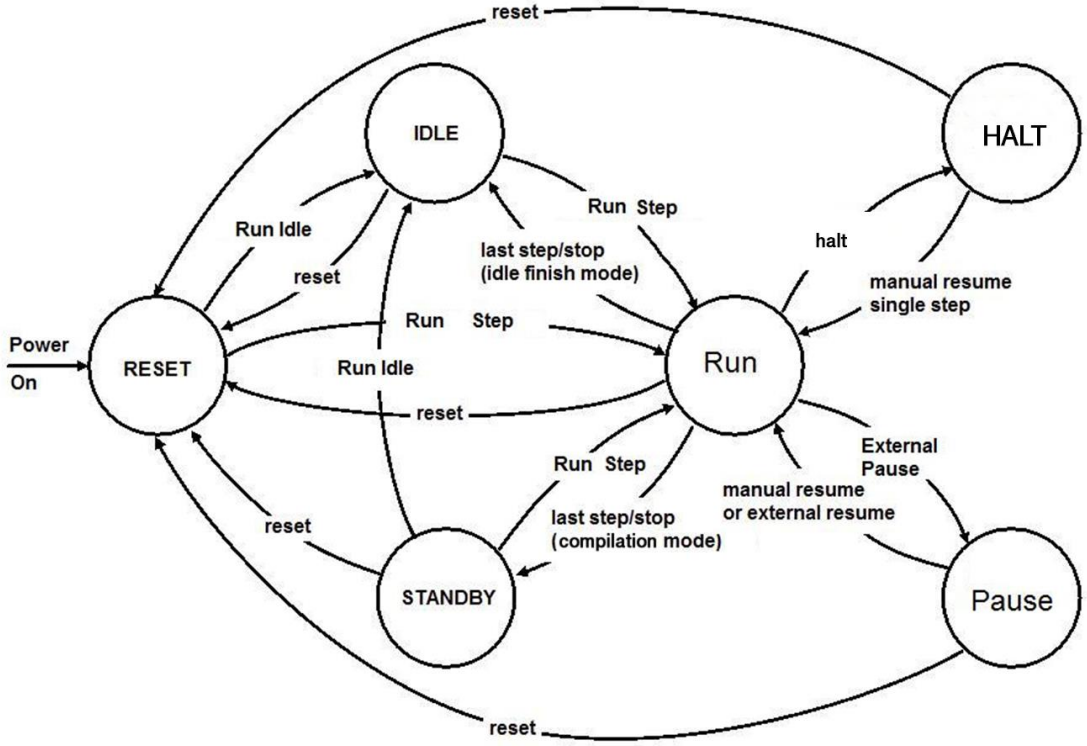

Figure 4-2: GX5296 Operational States

Reset State

When the sequencer is first powered, or goes through a **Reset** or **Sequencer Reset**, it is in the Reset State. In this state the sequencer is continuously looping on the first vector assigned to Step 0. All real-time compare errors are cleared and the sequencer is ready to enter another state.

Idle State

The sequencer will continuously run through all Vectors assigned to the Idle Step. During this time, the Vector Memory is busy and cannot be accessed by the User. The Idle state can be entered when a Run ends or is stopped manually by the user. It can also be entered manually by the user, before entering the Run State.

Standby State

The sequencer will run only the first Vector of the selected Finish Step. The Standby State is entered when a Run ends or is stopped manually by the user. The Standby State allows the user to maintain UUT stimulation between Digital Bursts.

Run State

The Run State is the primary execution state. The Run State can be entered manually, by user command or through an external trigger. The sequencer will run through each Step and execute each Vector assigned to the respective Step. The Vector Memory is busy during this state and it cannot be accessed by the User.

Halt State

The Halt State is entered through manual intervention by the user. The different Software Halt modes can be set by the user to allow different behaviors to occur when a Software Halt is commanded by the user. During the Halt state, the last Vector is output statically on the I/O channels.

Pause State

The Pause State is entered through external triggering or Pause signals. The Pause State is similar to the Halt State and is controlled by the current Pause Mode.

Finish/Idle State

One of the unique features of the GX5296 is the Finish/Idle state. After the execution of a burst, the sequencer will enter the Idle/Standby state. The user can define the Finish/idle state timing and vector such that UUT stimulus can be maintained between vector bursts. A single vector can be specified so that the vector memory can be updated (Finish) or a group of vectors can be specified (Idle) during this state.

The user can disable the timing set phases/windows during the Finish/Idle state by setting Assert/Return and Open/Close values to zero. See **GtDio6xSequencerSetFinishStep** in the Functions Reference chapter for information.

The following table describes the six execute states of the Gx5296 and how the state is entered:

Setting	Description	Entry Condition
RESET	Idle Active: false Sequence Active: false Halt flag: false Paused flag: false Active step: 0 Pattern Memory: Accessible	Power On Reset (**GtDio6xReset** API)
STANDBY	Idle Active: false Sequence Active: false Halt flag: false Paused flag: false Active step: User Pattern Memory: Accessible	Stop (**GtDio6xSequencerStop** API) Last Step standby completion mode (**GtDio6xSequencerSetRunCompletionMode** API)
IDLE	Idle Active: true Sequence Active: false Halt flag: false Paused flag: false Active step: User Pattern Memory: Busy	Run idle (**GtDio6xSequencerRunIdleStep** API) Stop (**GtDio6xSequencerStop** API) Last Step completion mode (**GtDio6xSequencerSetRunCompletionMode** API)
RUN	Idle Active: false Sequence Active: true Halt flag: true Paused flag: false Active step: User Pattern Memory: Accessible	Run (**GtDio6xSequencerRun** API) Resume (**GtDio6xSequencerResume** API)
HALT	Idle Active: false Sequence Active: true Halt flag: true Paused flag: false Active step: User Pattern Memory: Accessible	Halt (**GtDio6xSequencerHalt** API)
PAUSE	Idle Active: false Sequence Active: true Halt flag: false Paused flag: true Active step: User Pattern Memory: Busy	Pause (**GtDio6xStepSetPauseResumeTrigger** API)

Table 4-3: Execute State Description

Clocks

The Gx5296 system uses several clocking signals to generate and capture digital vectors from the I/O Channels.

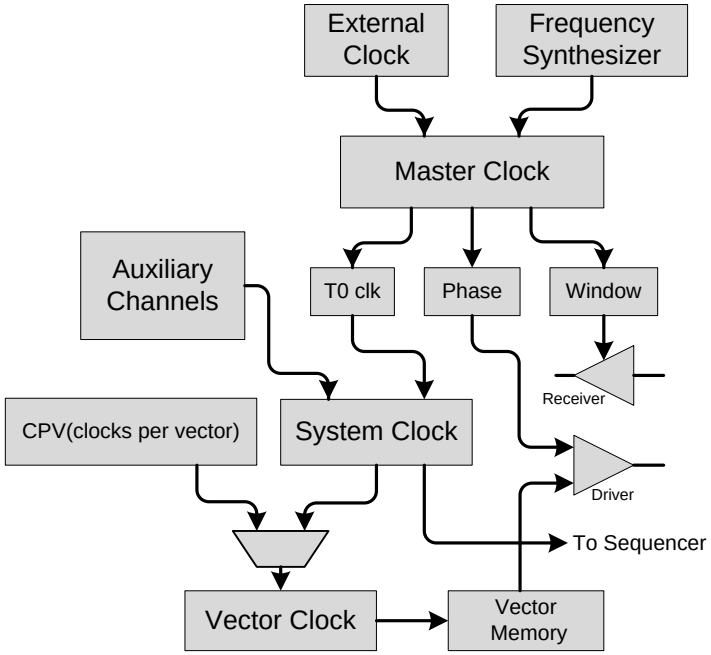

Figure 4-4: Clock Architecture Overview

Master Clock

The master clock defines the edge or timing resolution. This block contains a fixed 500 MHz master clock oscillator and a Frequency Synthesizer (FS) which may be used in lieu of the 500 MHz oscillator. The reference clock for the Frequency Synthesizer may be the built-in 20 MHz oscillator, 10 MHz PXI clock or an external oscillator in the range of 5 to 80 MHz.

Source	Description
500 MHz	Sequencer (timing) resolution set to 1ns
Frequency Synthesizer	Sequencer resolution set to 1 / (2 * FS) For example, if FS = 100 MHz Resolution = 1 / (2 * 100,000,000) Resolution = 5ns

Table 4-5: Master Clock Source Settings

See **GtDio6xSequencerSetMasterClockSource** in the functions reference chapter for information.

System Clock

The System Clock is used to apply Step settings (such as Phase, Window, and T0 Clock) to the sequencer. The System Clock also generates the Vector Clock which is used to define a Vector's period.

Source	Description
Internal T0 Clock	System Clock driven by the internal T0 Clock which is programmed per Step.
AUX0-AUX11	System Clock driven by the external auxiliary channels.
Frequency Synthesizer	System Clock driven by the internal frequency synthesizer signal.

Table 4-6: System Clock Source Settings

The relevant API function is: **GtDio6xSequencerSetSystemClockSource**

Vector Clock

The Vector Clock is derived from the System Clock and the Clocks per Vector setting. The Vector Clock period will equal the System Clock Period divided by the Clocks per Vector setting. The Vector Clock is used to clock out Vectors from memory when the Sequencer is running.

See **GtDio6xStepSetClock** in the functions reference chapter for information.

Timing Sets

The GX5296 Timing Subsystem is comprised of the System Clock, the Vector Clock and a Timing Generator which generates the Phase Assert, Phase Return, Window Open, and Window Close signals. The System Clock Cycle determines the base frequency at which Vectors are assigned to the currently running Step which will be clocked from the Vector Memory. The Vector Clock is derived from the System Clock, and is controlled by the Clocks per Vector setting. The Vector Clock period is equal to the System Clock period multiplied by the **Clocks per Vector**. The Phase and Window signals determine how and when (in conjunction with the Data Format) a Vector's output state will be applied to the I/O Pins within a System /Vector Clock cycle. The Phase Reset Source setting determines which clock (System or Vector) will cause the Phase signal to reset and begin again.

A timing set consists of four pair of Phase Asserts/ Phase Return and Window Open / Window Close. The timing sets are used to control the channel drivers and receivers.

Phase

A Phase controls the driver output operation and consists of an Assert and a Return edge. The Assert signal loads the current pattern code in to the output driver. The Return signal is used to enable the format code in the driver. The Return signal is not used for the Non Return format code.

Window

The Window controls the signal capture for the receiver and consists of an Open and Close edge. Each channel can be set to one of three capture modes. In Windowed mode, the Window Open signal begins signal capture and the Window Close ends the capture. In Open Edge mode, the Window Open edge strobes the channel comparator input and the Close Edge is ignored. In Close Edge mode, the Window Close edge strobes the channel comparator input and the Open Edge is ignored.

The Phase timing logic can be triggered by either the System Clock or the Vector Clock. The Window timing logic is triggered by the Vector Clock.

A timing diagram of the System Clock, Vector Clock, Window, and Phase signals is shown in Figure 4-4.

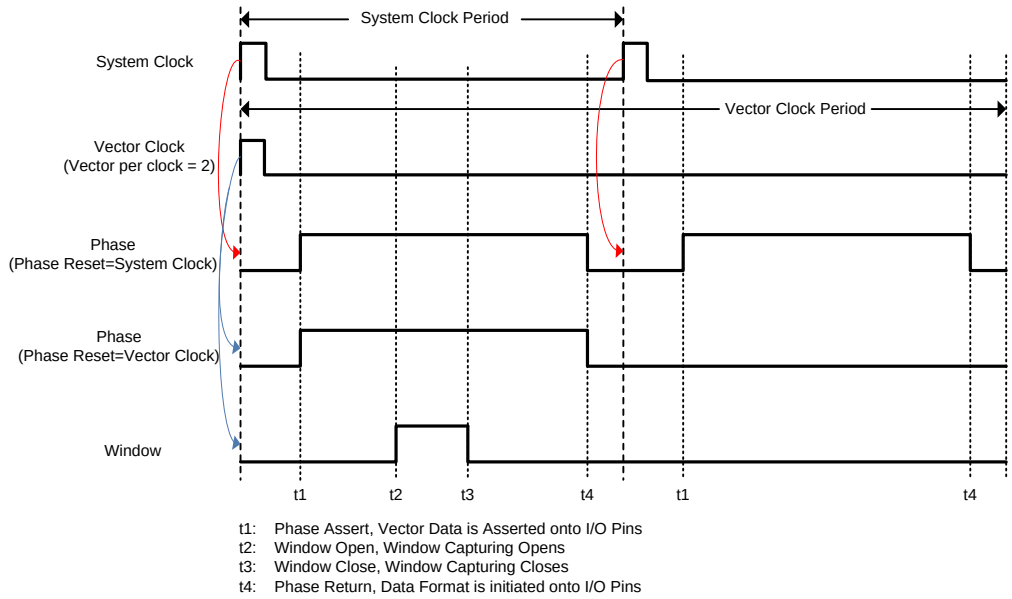

Figure 4-7: System Clock, Vector Clock, Phase and Window Timing Diagram

Indexed Timing Sets

Timing Sets are used in Indexed Timing Sets mode which consists of 4096 Steps, each Step can be programmed to point to any of the 64 timing set located in the Timing Set Index Memory. Each timing set is composed of four pairs of Phase and Window settings as follows:

Timing Set Index Number	TSet 0: First pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 0 Phase Return 0 Window Open 0 WindowClose 0
	TSet 1: Second pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 1 Phase Return 1 Window Open 1 WindowClose 1
	TSet 2: Third pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 2 Phase Return 2 Window Open 2 WindowClose 2
	TSet 3: Fourth pair of Phase and Window in the specified Timing Set Memory Index	Phase Assert 3 Phase Return 3 Window Open 3 WindowClose 3

Table 4-8: Componenets of a single Timing Set

The user can assign one of the four timing set's Index number to any I/O channel or a range I/O channels. The Timing Set to I/O channel assignment relationship will be maintained and applied to every Step / Timing Set in Step Memory. Timing set index is programmed per Step. Each channel can be set to use any of the four Phase Assert and Phase Return pair, as well any of the Window Open and WindowClose pairs. E.g. Channel 1 can have TSet 0 for Phase Assert and Phase Return, and TSet 2 as the Window Open and WindowClose. Each step can be assign one of the 64 Timing Set Index numbers, while the channels will maintain the Phase and Window TSet settings.

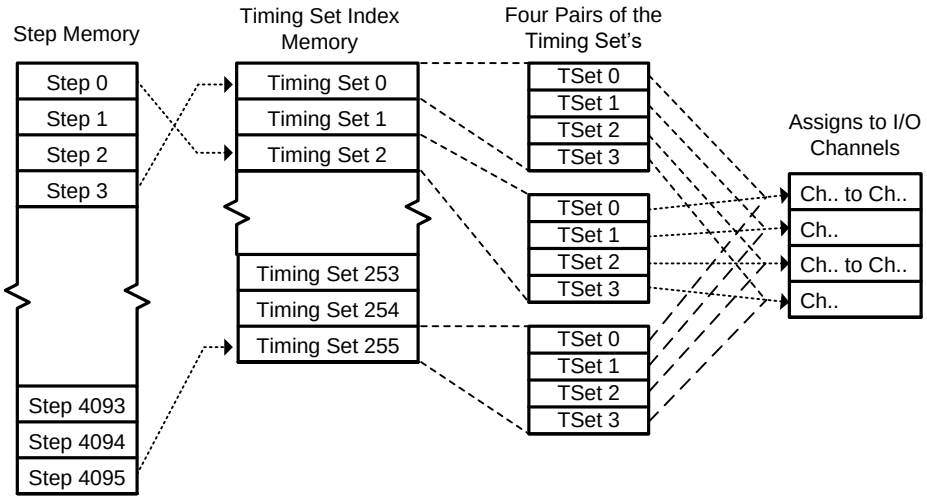

Figure 4-9: Indexed Timing Sets Diagram

Vector Memory

The Gx5296 has a unified Vector memory which combines several pieces of information. Each Vector channel state is represented in the form of an ASCII character. The ASCII Character encodes the Output, Real Time Expect, Tristate Control (Direction), and Mask information for a particular channel within a Vector. The Vector Memory API functions allow the user to write and read from Vector Memory to any desired channel or group of channels for a given range of Vectors.

A separate Record Memory contains either response data or error data depending on the Record Mode selected for a particular Step. If the Step's Record Mode is set to Response, a '1' indicates a logic high response, and a '0' indicates a logic low response. If the Step's Record Mode is set to Error, a '1' indicates a real time compare error, and a '0' means no real time compare error occurred. The Record Memory stores up to 64M of response vectors. The indices of the Record Memory are mapped 1 to 1 with the Vector Memory.

Opcode	Description	Driver State	Drive Level	Comparator Expect	Invert Code
1	Drive High, Don't Expect (Don't Care)	On	VoH	None	Drive Low '0'
0	Drive Low, Don't Expect (Don't Care)	On	VoL	None	Drive High '1'
h	Drive High, Expect High	On	VoH	>ViH	Drive Low, Expect Low 'l'
l	Drive Low, Expect Low	On	VoL	<ViL	Drive High, Expect High 'h'
H	Expect High, Don't Drive	Off	X	>ViH	Expect Valid Low 'L'
L	Expect Low, Don't Drive	Off	X	<ViL	Expect Valid High 'H'
Z	Tristate (Disabled)	Off	N/A	None	Disable Channel 'Z'
/	Drive Low, Expect High	On	VoL	>ViH	Drive High, Expect Low '\'
****	Drive High, Expect Low	On	VoH	<ViL	Drive Low, Expect High '/'
V	Expect Valid Level	Off	X	>ViH OR <ViL	Expect Invalid 'B'
B	Expect Invalid Level	Off	X	<ViH AND >ViL	Expect Valid 'V'
R	Repeat previous opcode	Repeats the last non repeat/invert code.			
I	Invert previous opcode	Inverts the last non repeat/invert code. Refer to Invert Code			
C	Collect CRC	Off	X	None	Collect CRC 'C'

Table 4-10: Vector Opcode Description Sequencer Step Memory

When running the Sequencer executes a series of one or more Steps, as defined by the user. This execution is known as a Burst. The Burst will continue until a non-jumping Step is executed with the Last Step flag set to True. At this point, the Sequencer will enter the Finish or Idle Step (see Finish/Idle State) A Step points to a block of vectors (contiguous, in vector memory) and applies timing, control, and record parameters during run-time.

Vector Assignment

Each Step can be assigned a block of vectors from the vector memory. The Step contains the number of vectors and the start offset (from Vector memory 0) address. Steps can have overlapping or identical vector assignments (offset location and number of Vectors). The number of vector s can be from 1 vector up to 67108864 (64M), for each step.

See **GtDio6xStepSetVectorCount** in the functions reference chapter for more information.

T0 Clock

The T0 Clock or System Clock is the programmable clock which is common to all the steps. The clock can be programmed to any value between 1000.0 nSec to 8.0 nSec, and the default is 100 nSec.

See **GtDio6xStepSetClock** in the functions reference chapter for more information.

Timing

Each Step is accoicated with a Timing Set Index Memory location. That information Timing Set Index Memory location defines the Phase Assert/Return, and Window Open/Close timing sets in terms of nSec. The Timing Sets available per Step, and the way to configure them is described in the **Indexed Timing Sets** section of this chapter.

See **GtDio6xStepSetTimingSets, GtDio6xStepSetTimingSetIndex** for more information.

Clocks per Vector

Two clocks are available for triggering the vectors' phase and window timing sets, System Clock (T0 Clock) and Vector Clock.

The Clocks per Vector determines the number of System Clocks that will be generated for each Vector Clock. When Clocks per Vector = 1, the Vector Clock period is equal to System Clock period. When Clocks per Vector = 2, the Vector Clock period is two times the System Clock period.

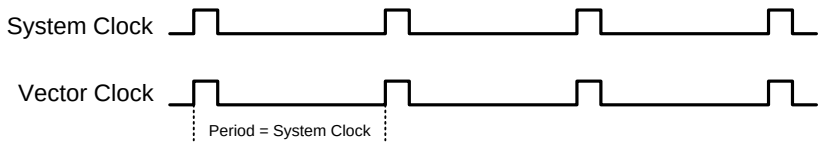

Figure 4-11: Timing Diagram of Clocks per Vector at 1

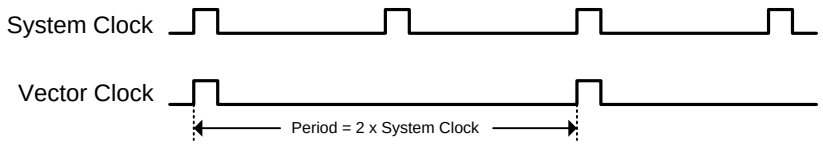

Figure 4-12: Timing Diagram of Clocks per Vector at 2

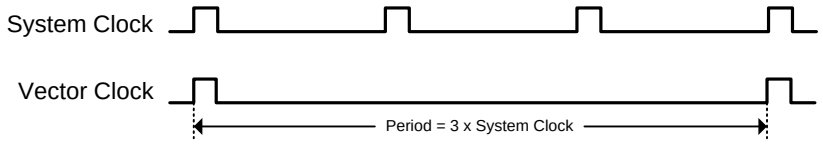

Figure 4-13: Timing Diagram of Clocks per Vector at 3

See **GtDio6xStepSetClock** for more information.

Record Mode

Each Step can be configured to use the Record Memory in a specific manner.

The Step can be configured to record a response or perform a real time compare of error states.

The user can also choose to not write to the record memory. The following describes the various record modes:

- None - All three record memories are disabled. The record memory does not record any incoming data. The record memory can either be set to record all zeros (No Error) or disabled using the **GtDio6xSetSequencerRecordMode** API.
- Record Count - The Error Count and Error Address Memory are enabled (See comments). The record memory does not record any incoming data. The record memory can either be set to record all zeros (No Error) or disabled using the **GtDio6xSetSequencerRecordMode** API.
- Record Error - All three memories are enabled, the Error Count and the Error Address Memory, the Record Index Memory and the Record Memory. The Record Memory is set to record real time record data.
- Record Response - All three memories are enabled. All three memories are enabled, the Error Count and the Error Address Memory, the Record Index Memory and the Record Memory. The Record Memory is set to record response data.

See **GtDio6xStepSetRecordMode** for more information.

Phase Reset Source

The phase reset source allows the user to select the phase reset signal source which can be the System Clock or the Vector Clock. The phase reset signal restarts the phase assert and return timing.

See **GtDio6xStepSetPhaseTriggerSource** for more information.

Last Step Flag

This flag indicates whether the current step is the last step of the sequence burst or a sub-step of a multi step burst.

See **GtDio6xStepSetLast** for more information.

Control Logic

There is one control statement that is evaluated at the end of each Step by the Sequencer. The control statement is part of the Step's memory structure. At the end of a Step (where one or more Vectors were executed), a control statement allows the Sequencer to Jump, Go to Subroutine, Loop, Stop, or Continue to the next Step. The branching can be made on the following conditions:

The selections are:

1. GTDIO6X_CONTROL_CONDITION_ALWAYS: Jump always (Unconditional).
2. GTDIO6X_CONTROL_CONDITION_RTC_ERROR_IN_STEP: Jumps if the Real Time Compare detected at least one failure in the step. See comments for details.
3. GTDIO6X_CONTROL_CONDITION_NO_RTC_ERROR_IN_STEP: Jumps if the Real Time Compare did not detect any failures in the step.
4. GTDIO6X_CONTROL_CONDITION_RTC_ERROR_COUNT_NOT_ZERO: Real Time Compare Error Count Not Zero (burst accumulated).
5. GTDIO6X_CONTROL_CONDITION_RTC_ERROR_COUNT_ZERO: RTC Error Count Zero (burst accumulated). Real Time Compare Error Count Zero (burst accumulated).
6. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_0_TRUE: Jump 0 Trigger True..
7. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_0_FALSE: Jump Trigger 0 False..
8. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_1_TRUE: Jump Trigger 1 True..
9. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_1_FALSE: Jump Trigger 1 False..
10. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_2_TRUE: Jump Trigger 2 True..
11. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_2_FALSE: Jump Trigger 2 False..

12. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_3_TRUE: Jump Trigger 3 True..
13. GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER_3_FALSE: Jump Trigger 3 False..

Two jump types can be set, Normal and Gosub.

- Jump: Forces the next sequence step number to be replaced by the specified step number.
- Gosub jumps save the current step number and forces the next sequence step number to be replaced by the specified step number. The Gosub Return flag set true will force the sequence step number to be one more that the saved step number. For example if step number 5 and 7 had a gosub to step 10 and step 13 has the gosub return flag set, then the step number sequence starting from 1 would be, 1, 2, 3, 4, 5, 10, 11, 12, 13, 6, 7, 10, 11, 12, 13, 8, 9, …

Jump Condition:

- GTDIO6X_CONTROL_CONDITION_RTC_ERROR_IN_STEP and GTDIO6X_CONTROL_CONDITION_NO_RTC_ERROR_IN_STEP: The sequence step jump logic includes a pass/fail condition. The pass/fail condition is the combination of all the valid channel comparator results and the condition enable flag for the current vector. The condition enable flag for the current vector is set by calling **GtDio6xWriteVectorTestFlagsMemory** API and can be enabled/disabled per vector. This pass/fail condition is then inserted in a 32 bit pipeline. The contents of the pipeline are ANDED with the contents of the pipeline mask to generate a pass/fail flag that the sequencer can jump on. Bit 0 is the mask for the first bit in the pipeline and bit 31 is the mask for the last bit in the pipeline. If no bits are set, raw error is used for jumping, counting burst errors and logging errors in the error address memory. See the **GtDio6xRealTimeCompareSetJumpPipelineMask** API for more details. At least one vector in the specified step has to have its condition vector flag be set. The Real Time Compare condition vector flag allows the user to determine if any of the expect pattern codes will cause the conditional jump pass/fail flag to be set if the expected state is not true. See **GtDio6xRealTimeCompareSetJumpSource** API.
- GTDIO6X_CONTROL_CONDITION_RTC_ERROR_COUNT_NOT_ZERO and GTDIO6X_CONTROL_CONDITION_RTC_ERROR_COUNT_ZERO: The error vector flag allows the user to determine if any of the expect pattern codes will cause the burst error flag to be set if the expected state is not true. At least one vector in the specified step has to have its error vector flag be set in order to enable the error count. See **GtDio6xRealTimeCompareSetJumpSource** API.
- GTDIO6X_CONTROL_CONDITION_JUMP_TRIGGER: Four sequence step jump triggers are available. The sequence step jump triggers are used for conditional jumping/looping. A jump/loop can be based on the true/false state of any of the four sequence step jump triggers. For example if jump trigger 1 test mode is set to 'Low Level', then a jump if trigger 1 true would occur if the selected jump trigger 1 source is low. See the **GtDio6xTrigConfigSetJumpTrigger** API for more details. The true/false state of the jump triggers is based on the jump trigger test event. If the jump trigger event is set to “Low Level”, then true would indicate the jump trigger signal is low and false would indicate the jump trigger signal is high.

See **GtDio6xStepSetControl** for more information.

Record Memory

A separate Record Memory contains either response data or error data depending on the Record Mode selected for a particular Step. If the Step’s Record Mode is set to Response, a ‘1’ indicates a logic high response, and a ‘0’ indicates a logic low response. If the Step’s Record Mode is set to Error, a ‘1’ indicates a real time compare error, and a ‘0’ means no real time compare error occurred. The Record Memory can store up to 64M response vectors. The indices of the Record Memory are mapped 1 to 1 with the Vector Memory.

Test Logic

The Test Logic circuit consists of Control Resources and Triggers which are used to provide the sequencer with testable conditions by which a certain action can be taken.

Control Resource

A Control Resource is a user configurable signal which is tested in the Test Logic block; the results of the test are used by the Sequencer during the execution of the control statement at the end of each Step. There are four selectable Control Resources (0, 1, 2, 3); the following input signal sources can be assigned to any one of the four Control Resources:

- Aux Channels 0 to 11
- Channel Comparet 0
- PXI Trigger 0 to 7.

The Control Resource tests the assigned input signal (the source signal can also be inverted before testing) for one of the following actions:

- Low Level.
- High Level.
- Rising Edge.
- Falling Edge.

The generated Control Resource signal is used in the Step's control statement as a conditional Boolean to determine if a Jump or Loop should occur.

There is a Reset Mode that controls how and when the Control Resource signal is reset to a low:

- Reset at the start of a Burst.
- Reset at the start of a Step.
- Reset at the start of a Step and when resuming a paused Sequencer.

See **GtDio6xTrigConfigSetJumpTrigger** for more information.

Triggers

A Trigger is a user configurable signal which is tested in the Test Logic block; the results of the test are used by the Sequencer during execution to perform an action such as Run, Stop, or Pause. There are three Trigger available:

- Run Trigger
- Stop Trigger
- Pause Trigger

There are several selectable Trigger sources; these source signals can be inverted before being tested. The following input signal sources can be assigned to be a Trigger signal:

- Aux Channels 0 to 11
- Channel Compare 0
- PXI Trigger 0 to 7.

Once the Trigger source is selected, the Trigger signal can be tested in one of the following ways:

- Low Level
- High Level
- Rising Edge
- Falling Edge

There is a Reset Mode that controls how and when the Trigger Resource signal is reset to low:

- Reset at the start of a Burst.
- Reset at the start of a Step.

See GtDio6xSetTrigger for more information.

Channel Compare

There are 4 Channel Compare signals (Channel Compare 0 to Channel Compare 3) per DIO board.

A Channel Compare is a configurable, active-low, signal that evaluates the levels of all I/O Channels of a DIO board against an expected pattern and a mask. If the I/O Channel levels (that are not masked out) match the expected pattern, the Channel Compare signal will transition from a high to a low and remain low until the I/O Channel levels no longer match the expected pattern. The **Channel Compare 0** signal can be used as a source for the Triggers and Control Resource. All Channel Compares can be connected (provide output) to the Auxiliary Channels of a domain.

See GtDio6xSequencerSetChannelsCompareTrigger for more information.

I/O Channel Operation

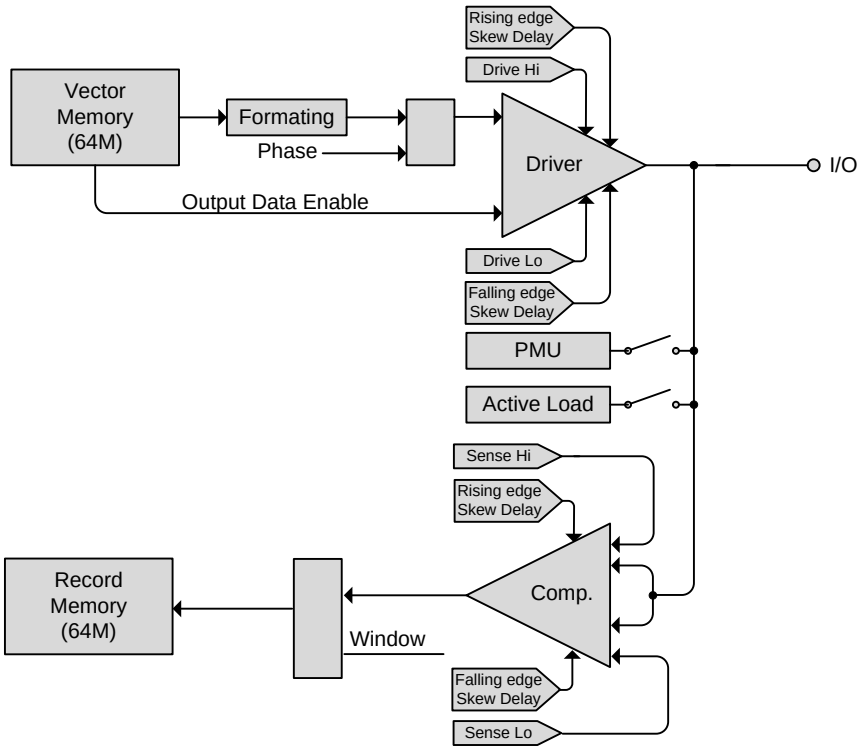

Figure 4-14: I/O Channel Block Diagram

Figure 4-6 is a block diagram of a single I/O pin. Up to 20 boards can be used in one domain for a maximum of 640 pins (each board containing 32 I/O pins). Output data, which is stored in the Vector memory, is outputted from the board as a function of the PHASE signal through the Driver when enabled; the encoded data (see Memory Management) enables the Driver output when the specified Vector is defined as an output Vector. The output data to the UUT will also be stored in the Record memory via the receiver pin electronics. The output data will be formatted as it was defined programmatically by the user to one of the following formats: No Return, Return to Zero, Return to One, Return to Hi-Z, Return to Complement, Surround Complement.

Each data channel's output signal has programmable Drive Out Hi and Drive Out Lo levels. The Drive Out Hi level can be set from -2 volts to +7 volts and must be greater than the output driver's Drive Out Low voltage. The Drive Out Low voltage can be set from -2 volt to +7 volts.

Each Driver has output over current protection. Once an over current condition occurs, the output will be set automatically to Hi-Z impedance. The over current event can be monitored by the CPU as well as cleared under CPU control in order to re-enable the output.

The pin electronics input analog stage is comprised of a set of constant current sink and source loads, and clamping (commutation) sink and source voltages. In addition, the input channel programmable load can be set to have constant source and sink current loads up to 24 mA each with 0.3662 µA of resolution. The input channel's current source will force the specified constant current to be active when the input voltage is above the high voltage clamp value. The input channel's current sink forces the specified constant current to be active when the input voltage is below the low voltage clamp value.

The input signal is connected to two comparators. The threshold sense high and low voltage levels are set programmatically by the user. Both the input high and low voltage threshold values can be set from -2.0V to +7.0V. Each channel's operating temperature, drive high / drive low voltages, sense hi / sense lo voltages, and output current values can all be monitored and measured.

Input data is stored in the Record Memory and is stored at the rate of the Vector Clock. The Vector opcode, once decoded, (see Memory Management) enables the input when the specified step is defined as an input step.

The input data will be processed as follows:

- If input data is higher than the high voltage threshold, the input is detected as logic high. Data will be logged as logic high to the input memory and a 0 is logged to the valid data memory.
- If input data is lower than the low voltage threshold, the input is detected as a logic low. Data will be logged as a logic low to the input memory and a 0 is logged to the valid data memory.
- If input data is higher than a low voltage threshold and lower than a high voltage threshold, input is invalid. Data will be logged as a logic low to the input memory and logged as a 1 to the invalid data memory.

Note: Each channel's output and input are connected. As a result whenever a channel is defined as an output for a specified step, it will be recorded to the In Memory while running.

Programmable Input Current Load and Voltage Clamps

Each channel has a constant current source and sink load currents and a corresponding voltage clamp that can be set and enabled programmatically. The constant current source and sink load currents are enbled only when the specified channel's driver state is Off. The following Opcodes will activate the active load (if it was enabled through the driver prior to runnig):

Opcode	Description	Driver State	Drive Level	Comparator Expect	Invert Code
H	Expect High, Don't Drive	Off	X	>ViH	Expect Valid Low 'L'
L	Expect Low, Don't Drive	Off	X	<ViL	Expect Valid High 'H'
Z	Tristate (Disabled)	Off	N/A	None	Disable Channel 'Z'
V	Expect Valid Level	Off	X	>ViH OR <ViL	Expect Invalid 'B'
B	Expect Invalid Level	Off	X	<ViH AND >ViL	Expect Valid 'V'
C	Collect CRC	Off	X	None	Collect CRC 'C'

The input channel's current load will provide a constant current sink when the input voltage is above the specified commutating voltage, and will provide a constant current source when the input voltage is below the specified commutating voltage. The constant current source and sink values can be set from 0mA to 24mA with 0.3662 µA of resolution.

The input channel's source and sink constant currents can be read back and set dynamically at any time even when the DIO is in its run state.

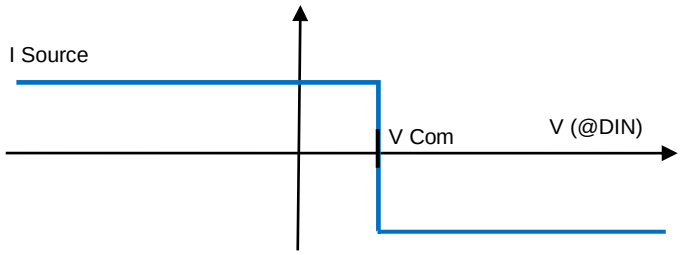

Figure 4-15: GX5296 Input Load Current Voltage Clamps

Sense Voltages

Each channel has a high-speed dual voltage comparator with its own independent threshold setting. Each channel's high and low input voltage threshold comparators can be set programmatically. There are two threshold voltage level settings for each input channel: logic high level and logic low level. Each input channel can detect three voltage levels: High, low and undefined. When the input voltage is equal or greater than the threshold logic high, a logic high is recorded. When the input voltage is equal or less than the threshold logic low, a logic low is recorded. When the input voltage is between the threshold high level and the threshold low setting then the value is recorded as an in-valid logic level.

The input high and input low voltage thresholds can operate over a range from -2V to +7V with the high threshold higher than the input low voltage threshold and the low voltage threshold lower than the input high voltage threshold.

The Input channel's low and high threshold voltages can be read back and set dynamically at any time even when the DIO is in the run state.

Output Data Formatting

Each output channel's data can be formatted as follows:

No Return	The output logic level stays either high or low for the duration of the clock period (default).
Return to Zero	The signal returns to zero during the phase return edge within a clock cycle.
Return to One	The signal returns to one during the phase return edge within a clock cycle.
Return to Hi-Z	The signal returns to Hi-Z during the phase return edge within a clock cycle.
Return to Complement	The Return to Complement (also called Manchester code) format ensures that each transmitted data bit has at least one transition during the phase return edge within a clock cycle. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. Return to Complement ensures frequent data transitions which are directly proportional to the clock rate which helps clock recovery. A logic low is expressed by a low-to-high transition. A logic high is expressed by high-to-low transition. The transitions which signify logic high or low occur at the midpoint of a period, the direction of the mid-bit transition indicates the data.
Compliment Surround	Tristate driver from beginning of vector to assert time and then drive programmed level. Tristate driver at return time.
Force Zero	Force driver to low level
Force One	Force driver to high level
Force Off	Force driver to Hi-Z
Force Inverted Phase	Drive high to low at the phase assert edge and low to high at the phase return edge.
Force Phase	Drive low to high at the phase assert edge and high to low at the phase return time.

Note: the specified channel data format will be applied to all the channels' vectors that are set as outputs. The inputs do not support or decode formatted data.

PMU Functionality

Each digital channel includes a parametric measurement unit (PMU) which can be used to characterize and measure a digital pin's DC characteristics. The PMU can be configured for force current, measure voltage, or force voltage, measure current. The PMU's range of operation is listed below:

Force voltage: -2 volts to +7 volts.

Measure voltage: -2 volts to +7.

Force curent: +/- 32 mA FS, +/- 8 mA FS, +/- 2 mA FS, +/- 512 uA FS, +/- 128 uA FS, +/- 32 uA FS, +/- 8 uA FS or +/- 2uA FS

Masure curent: +/- 32 mA FS, +/- 8 mA FS, +/- 2 mA FS, +/- 512 uA FS, +/- 128 uA FS, +/- 32 uA FS, +/- 8 uA FS or +/- 2uA FS

Measurement resolution is 16 bits for both voltage and current measurement functions. Note that while each channel has a dedicated PMU, the measurement resource is shared between all 32 channels, requiring sequential measurement of each channel.

Appendix A – Thermal and Power Considerations

Overview

The GX5296 is high performance PXI instrument and depending on specific operating conditions, the board can require significant power and cooling. The table below provides a summary of the GX5296's power requirements for static and dynamic operating conditions. Specific power requirements and dissipation will be dependent on the number of active digital channels and data rate. If using the board's PMU capabilities only, the board's power consumption is similar to the idle / initialized operating condition.

GX5296 Power Requirements

Operating Condition	+3.3 V	+ 5.0 V	+12 V	-12 V	Watts
Idle, initialized	4.8 A	1.48 A	0.25 A	0	26
100 MHz, checker pattern, VL= -1 V, VH= +7 V, no de-skew	8.6 A	5.0 A	0.44 A	0	58.6
100 MHz, checker pattern, VL= -1 V, VH= +7 V, with de-skew	9.7 A	5.0 A	0.44 A	0	62.4

Note: All PXI chassis are required to supply at least 30 watts of power per slot. For high performance applications or multiple card configurations, a PXI chassis needs to be selected that has adequate DC power and cooling capabilities such as the Geotest GX7300 or GX7600. A PXI peripheral slot can deliver 60 watts however; you must ensure that the PXI chassis has adequate DC power for your specific application and configuration.

Caution - The GX5296 can dissipate significant heat. It is essential that the PXI chassis' cooling system not be restricted and that all blank PXI slots be closed. Any air flow restrictions such as dirty air filters or blocked ventilation openings can result in excessive heat rise within the chassis and damage to the GX5296.

Index